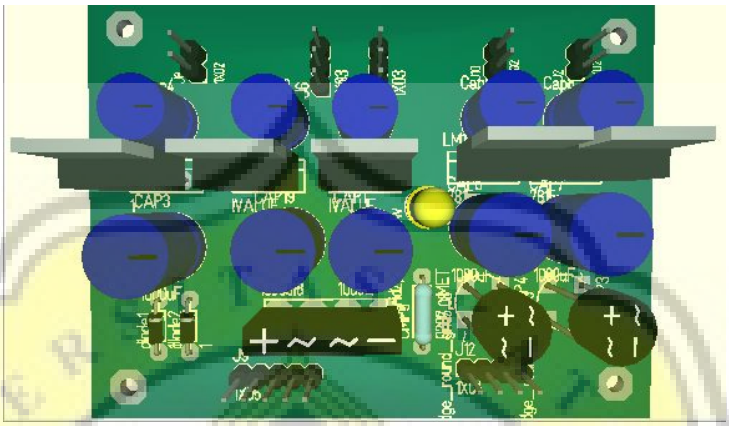
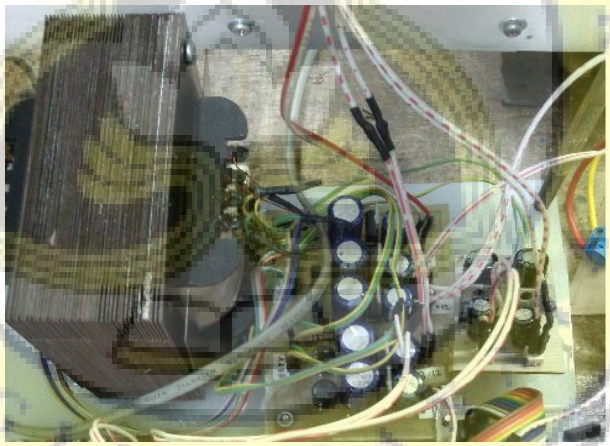
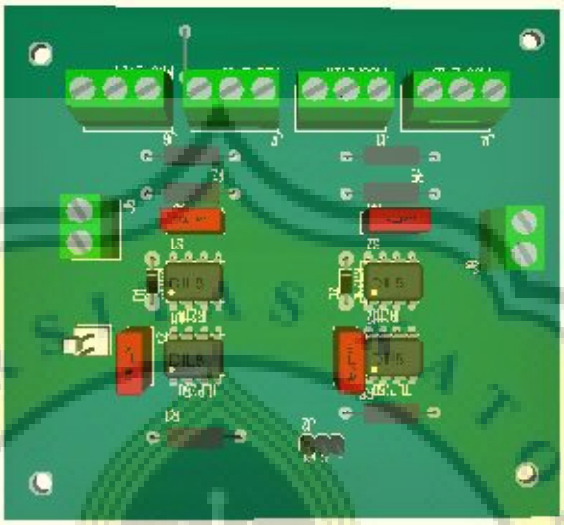
LAMPIRAN



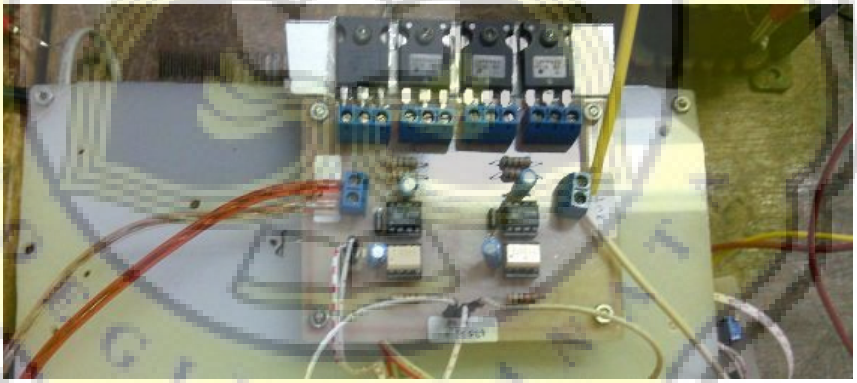
Hasil desain catu daya menggunakan target



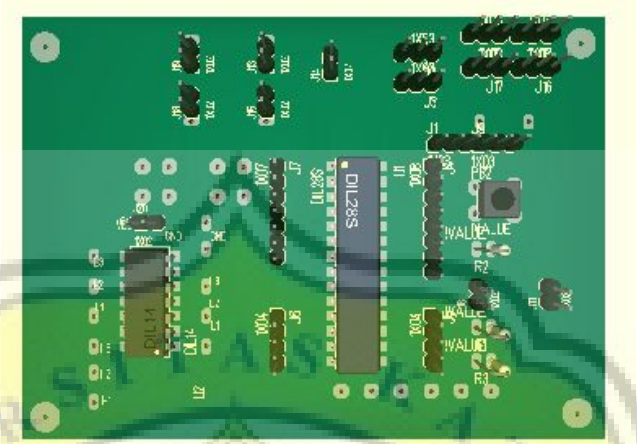
Hasil implementasi catu daya



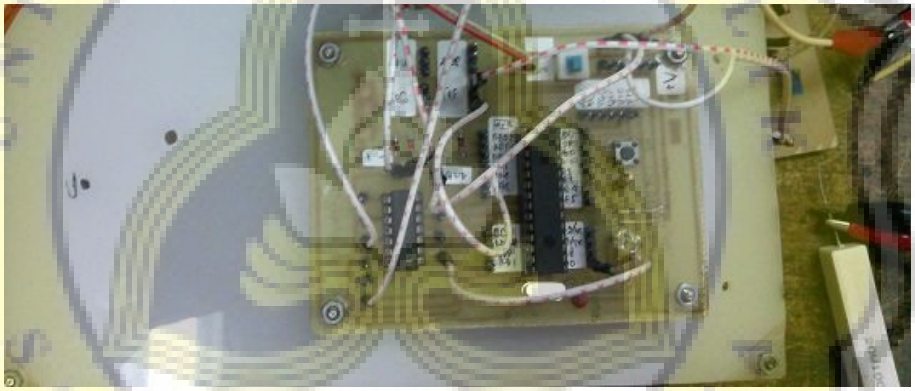
Hasil desain rangkaian daya dan penggerak dengan target



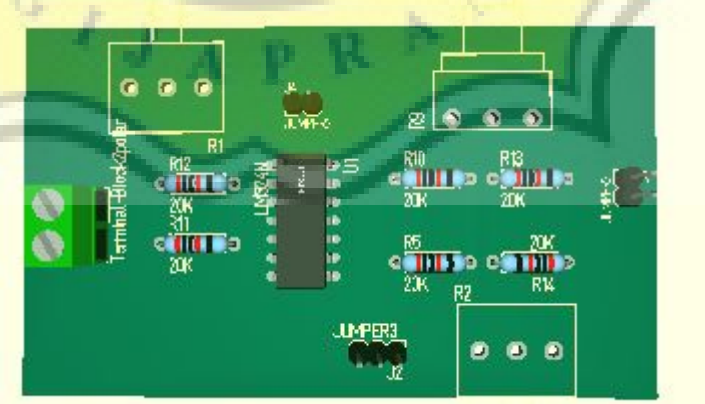
Hasil implementasi rangkaian daya dan penggerak



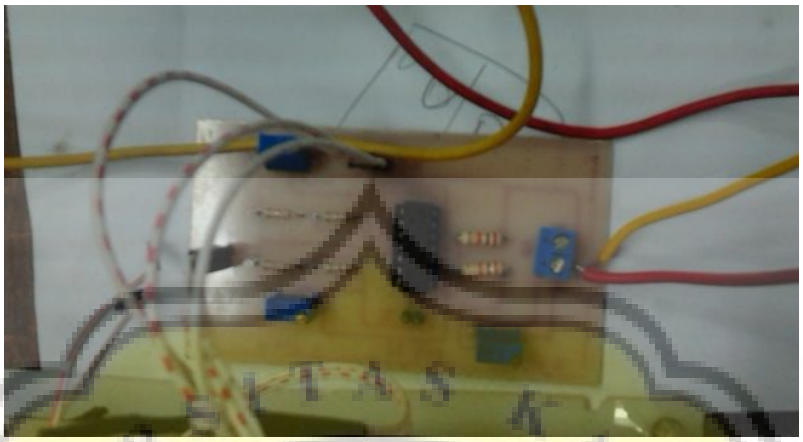
Hasil desain sismin kendali *dsPICC30F4012* dengan target



Hasil implementasi sismin kendali *dsPIC30F4012*

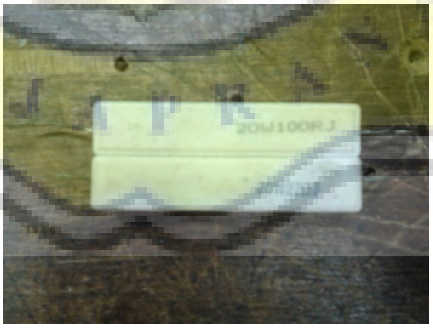


Hasil desain pendeteksi sinyal dengan target



Hasil implementasi pendeteksi sinyal

induktor



Beban resistor

Listing program kendali *dsPIC30F4012*

```
/*
=========================================================
 PROJECT = inverter
 Pendeteksi sinyal = RB3
 OUTPUT TO GATE = LATD
 Test configuration  MCU  :   dsPIC30F4012  (8 MHz)
=========================================================
*/

unsigned ADCvalue2,ADCvalue3,Reff,Error,Error1;
void Timer1Int() iv IVT_ADDR_T1INTERRUPT
{
T1IF_bit = 0;                        // Clear T1IF
ADCON1bits.SAMP = 1;
IFS0bits.ADIF = 0;                   // clear interrupt
while (IFS0bits.ADIF);               // conversion done?
{
ADCvalue2 = ADCBUF0;
ADCvalue3 = ADCBUF1;
}
   Reff    = ADCvalue3;              // baca pengolah sinyal
   Error   = Reff ;                  // pembuatan error
```

```
   Error1  = Error*2;
}
void main()
{
 TRISD = 0;
 TRISC = 0;

 LATD=0;
 LATC=0;

 ADPCFG = 0xFFF3;              // RB2 & RB3 = analog
 ADCON1 = 0x00E0;              // SIMSAM bit = 0 : Samples multiple channels individually in sequence
                               // ASAM = 0 : Sampling begins when SAMP bit set
                               // SSRC = 111 auto-convert
 ADCHS = 0x0302;               // Connect AN3 as CH0 input (MUXB) and AN2 as CH0 (MUXA)
 ADCSSL = 0;
 ADCON3 = 0x0302;              // Auto Sampling 3 Tad, Tad = internal 2 Tcy
 ADCON2 = 0x6005;              // Eksternal Vref
                               // only sample CH0
                               // SMPI = 0001 for interrupt after 2 converts
                               //MUXA and MUXB alternate
 ADCON1bits.ADON = 1;          // turn ADC ON
```

```
  IPC0   = IPC0 | 0x1000;              // Interrupt priority level = 1
  T1IF_bit = 0;                    // Clear T1IF
  T1IE_bit = 1;                    // Enable Timer1 interrupts
  T1CON = 0x8000;                   // Timer1 ON, internal clock FCY, prescaler
  PR1 = 2046;                       //MENGATUR PERIODE TIMER (200uS ' 5
kHz)



  while (1)
      {
          if (Error1 >= TMR1)        // komparasi Reff dengan carr
              RD0_bit = 1;
              else
              RD0_bit = 0;
}
}
```

Data sheet TLP 250

TOSHIBA Photocoupler GaAlAs Ired & Photo-IC

TLP250

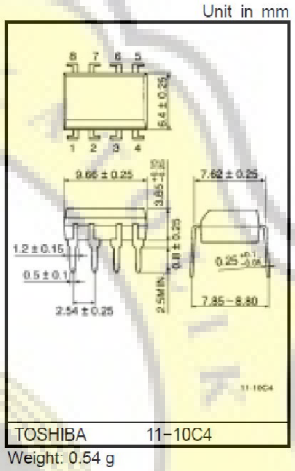
Transistor Inverter
Inverter For Air Conditionor
IGBT Gate Drive
Power MOS FET Gate Drive

The TOSHIBA TLP250 consists of a GaAlAs light emitting diode and a integrated photodetector.
This unit is 8-lead DIP package.
TLP250 is suitable for gate driving circuit of IGBT or power MOS FET.

- Input threshold current: I_F=5mA(max.)
- Supply current (I_{CC}): 11mA(max.)
- Supply voltage (V_{CC}): 10-35V
- Output current (I_O): ±1.5A (max.)
- Switching time (t_{pLH}/t_{pHL}): 1.5μs(max.)
- Isolation voltage: 2500V_{rms}(min.)
- UL recognized: UL1577, file No.E67349
- Option (D4) type
  VDE approved: DIN VDE0884/06.92,certificate No.76823
  Maximum operating insulation voltage: 630V_{PK}
  Highest permissible over voltage: 4000V_{PK}

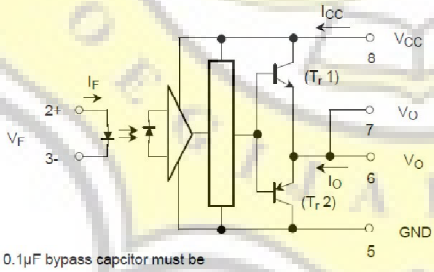
  (Note) When a VDE0884 approved type is needed, please designate the "option (D4)"
- Creepage distance: 6.4mm(min.)
  Clearance: 6.4mm(min.)

Unit in mm



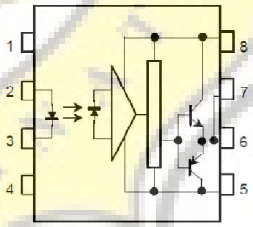
TOSHIBA 11-10C4
Weight: 0.54 g

Schmatic



A 0.1μF bypass capcitor must be connected between pin 8 and 5 (See Note 5)

Pin Configuration (top view)



1 : N.C.
2 : Anode
3 : Cathode
4 : N.C.
5 : GND
6 : V_O (Output)
7 : V_O
8 : V_{CC}

Truth Table

		Tr1	Tr2
Input LED	On	On	Off
	Off	Off	On

Absolute Maximum Ratings (Ta = 25°C)

	Characteristic		Symbol	Rating	Unit
LED	Forward current		I_F	20	mA
	Forward current derating (Ta ≥ 70°C)		$\Delta I_F / \Delta Ta$	−0.36	mA / °C
	Peak transient forward curent	(Note 1)	I_{FPT}	1	A
	Reverse voltage		V_R	5	V
	Junction temperature		Tj	125	°C
Detector	"H"peak output current (P_W ≤ 2.5μs,f ≤ 15kHz)	(Note 2)	I_{OPH}	−1.5	A
	"L"peak output current (P_W ≤ 2.5μs,f ≤ 15kHz)	(Note 2)	I_{OPL}	+1.5	A
	Output voltage	(Ta ≤ 70°C)	V_O	35	V
		(Ta = 85°C)		24	
	Supply voltage	(Ta ≤ 70°C)	V_{CC}	35	V
		(Ta = 85°C)		24	
	Output voltage derating (Ta ≥ 70°C)		$\Delta V_O / \Delta Ta$	−0.73	V / °C
	Supply voltage derating (Ta ≥ 70°C)		$\Delta V_{CC} / \Delta Ta$	−0.73	V / °C
	Junction temperature		Tj	125	°C
Operating frequency		(Note 3)	f	25	kHz
Operating temperature range			T_{opr}	−20~85	°C
Storage temperature range			T_{stg}	−55~125	°C
Lead soldering temperature (10 s)		(Note 4)	T_{sol}	260	°C
Isolation voltage (AC, 1 min., R.H.≤ 60%)		(Note 5)	BV_S	2500	Vrms

Note 1: Pulse width P_W ≤ 1μs, 300pps

Note 2: Exporenential wavefom

Note 3: Exporenential wavefom, I_{OPH} ≤ −1.0A(≤ 2.5μs), I_{OPL} ≤ +1.0A(≤ 2.5μs)

Note 4: It is 2 mm or more from a lead root.

Note 5: Device considerd a two terminal device: Pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.

Note 6: A ceramic capacitor(0.1μF) should be connected from pin 8 to pin 5 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching proparty. The total lead length between capacitor and coupler should not exceed 1cm.

Recommended Operating Conditions

Characteristic		Symbol	Min.	Typ.	Max.		Unit
Input current, on	(Note 7)	$I_{F(ON)}$	7	8	10		mA
Input voltage, off		$V_{F(OFF)}$	0	—	0.8		V
Supply voltage		V_{CC}	15	—	30	20	V
Peak output current		I_{OPH}/I_{OPL}	—	—	±0.5		A
Operating temperature		T_{opr}	−20	25	70	85	°C

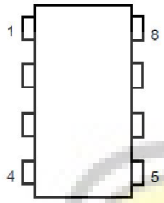
Note 7: Input signal rise time (fall time) < 0.5 μs.

Electrical Characteristics (Ta = −20~70°C, unless otherwise specified)

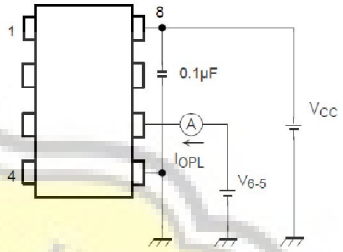
Characteristic		Symbol	Test Cir-cuit	Test Condition	Min.	Typ.*	Max.	Unit
Input forward voltage		V_F	—	I_F = 10 mA , Ta = 25°C		1.6	1.8	V
Temperature coefficient of forward voltage		$\Delta V_F / \Delta Ta$	—	I_F = 10 mA	—	−2.0	—	mV / °C
Input reverse current		I_R	—	V_R = 5V, Ta = 25°C		—	10	μA
Input capacitance		C_T	—	V = 0 , f = 1MHz , Ta = 25°C	—	45	250	pF
Output current	"H" level	I_{OPH}	3	V_{CC} = 30V (*1), I_F = 10 mA, V_{8-6} = 4V	−0.5	−1.5	—	A
	"L" level	I_{OPL}	2	V_{CC} = 30V (*1), I_F = 0, V_{6-5} = 2.5V	0.5	2	—	
Output voltage	"H" level	V_{OH}	4	V_{CC1} = +15V, V_{EE1} = −15V, R_L = 200Ω, I_F = 5mA	11	12.8	—	V
	"L" level	V_{OL}	5	V_{CC1} = +15V, V_{EE1} = −15V, R_L = 200Ω, V_F = 0.8V	—	−14.2	−12.5	
Supply current	"H" level	I_{CCH}	—	V_{CC} = 30V, I_F = 10mA, Ta = 25°C	—	7	—	mA
				V_{CC} = 30V, I_F = 10mA	—	—	11	
	"L" level	I_{CCL}	—	V_{CC} = 30V, I_F = 0mA, Ta = 25°C	—	7.5	—	
				V_{CC} = 30V, I_F = 0mA	—	—	11	
Threshold input current	"Output L→H"	I_{FLH}	—	V_{CC1} = +15V, V_{EE1} = −15V, R_L = 200Ω, V_O > 0V	—	1.2	5	mA
Threshold input voltage	"Output H→L"	I_{FHL}	—	V_{CC1} = +15V, V_{EE1} = −15V, R_L = 200Ω, V_O < 0V	0.8	—	—	V
Supply voltage		V_{CC}	—		10	—	35	V
Capacitance (input–output)		C_S	—	V_S = 0 , f = 1MHz, Ta = 25• •	—	1.0	2.0	pF
Resistance(input–output)		R_S	—	V_S = 500V , Ta = 25°C, R.H.≤ 60%	1×10^{12}	10^{14}	—	Ω

* All typical values are at Ta = 25°C (*1): Duration of I_O time ≤ 50μs

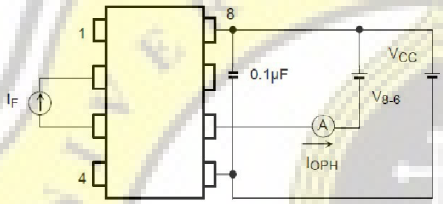
Test Circuit 1 :



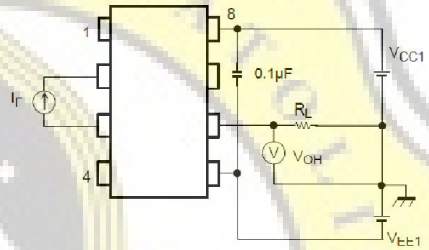
Test Circuit 2 : IOPL



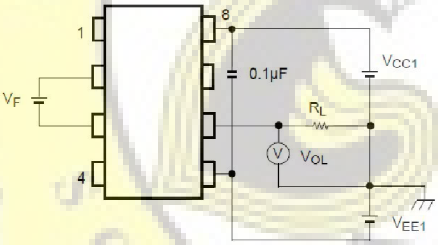
Test Circuit 3 : IOPH



Test Circuit 4 : VOH



Test Circuit 5 : V_{OL}



Data sheet IR2111

International
IOR Rectifier

Data Sheet No. PD60028-M

IR2111(S) & (PbF)

HALF-BRIDGE DRIVER

Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- CMOS Schmitt-triggered inputs with pull-down
- Matched propagation delay for both channels
- Internally set deadtime
- High side output in phase with input
- Also available LEAD-FREE

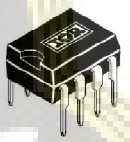
Product Summary

V_{OFFSET}	600V max.
I_O+/-	200 mA / 420 mA
V_{OUT}	10 - 20V
$t_{on/off}$ (typ.)	750 & 150 ns
Deadtime (typ.)	650 ns

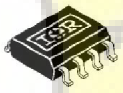
Description

The IR2111(S) is a high voltage, high speed power MOSFET and IGBT driver with dependent high and low side referenced output channels designed for half-bridge applications. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic input is compatible with standard CMOS outputs. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Internal deadtime is provided to avoid shoot-through in the output half-bridge. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

Packages

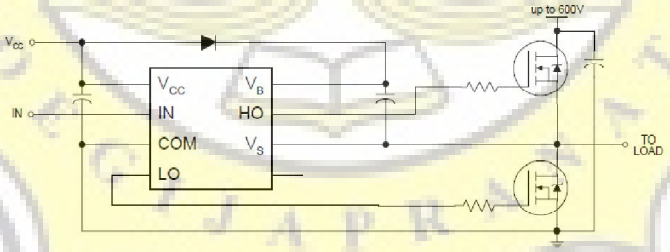


8-Lead PDIP



8-Lead SOIC

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in figures 7 through 10.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating supply voltage		-0.3	625	V
V_S	High side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage		-0.3	25	
V_{LO}	Low side output voltage		-0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage		-0.3	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient (figure 2)		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	(8 Lead PDIP)	—	1.0	W
		(8 lead SOIC)	—	0.625	
Rth_{JA}	Thermal resistance, junction to ambient	(8 lead PDIP)	—	125	°C/W
		(8 lead SOIC)	—	200	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	Note 1	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage	0	V_{CC}	
T_A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 pF and T_A = 25°C unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in figure 3.

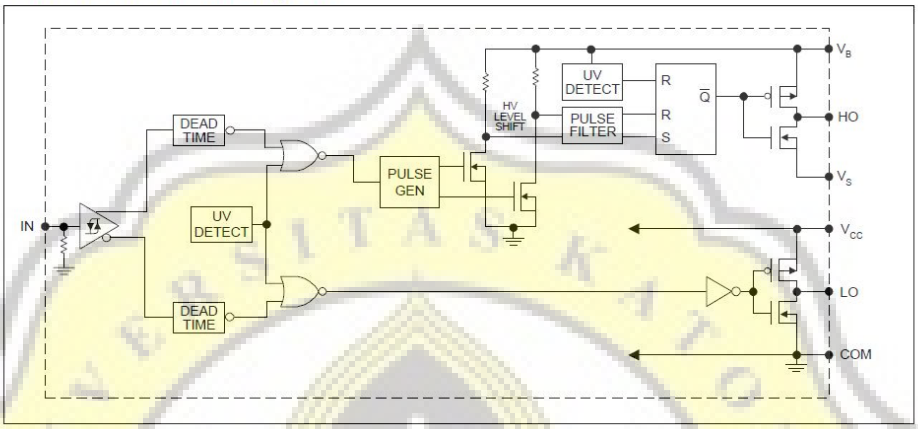
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	550	750	950	ns	V_S = 0V
t_{off}	Turn-off propagation delay	—	150	180		V_S = 600V
t_r	Turn-on rise time	—	80	130		
t_f	Turn-off fall time	—	40	65		
DT	Deadtime, LS turn-off to HS turn-on & HS turn-off to LS turn-on	480	650	820		
MT	Delay matching, HS & LS turn-on/off	—	30	—		

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage for HO & logic "0" for LO	6.4	—	—	V	V_{CC} = 10V
		9.5	—	—		V_{CC} = 15V
		12.6	—	—		V_{CC} = 20V
V_{IL}	Logic "0" input voltage for HO & logic "1" for LO	—	—	3.8		V_{CC} = 10V
		—	—	6.0		V_{CC} = 15V
		—	—	8.3		V_{CC} = 20V
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	—	100	mV	I_O = 0A
V_{OL}	Low level output voltage, V_O	—	—	100		I_O = 0A
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} supply current	—	50	100		V_{IN} = 0V or V_{CC}
I_{QCC}	Quiescent V_{CC} supply current	—	70	180		V_{IN} = 0V or V_{CC}
I_{IN+}	Logic "1" input bias current	—	30	50		V_{IN} = V_{CC}
I_{IN-}	Logic "0" input bias current	—	—	1.0		V_{IN} = 0V
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	7.6	8.6	9.6	V	
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	7.2	8.2	9.2		
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	7.6	8.6	9.6		
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	7.2	8.2	9.2		
I_{O+}	Output high short circuit pulsed current	200	250	—	mA	V_O = 0V, V_{IN} = V_{CC} PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	420	500	—		V_O = 15V, V_{IN} = 0V PW ≤ 10 µs

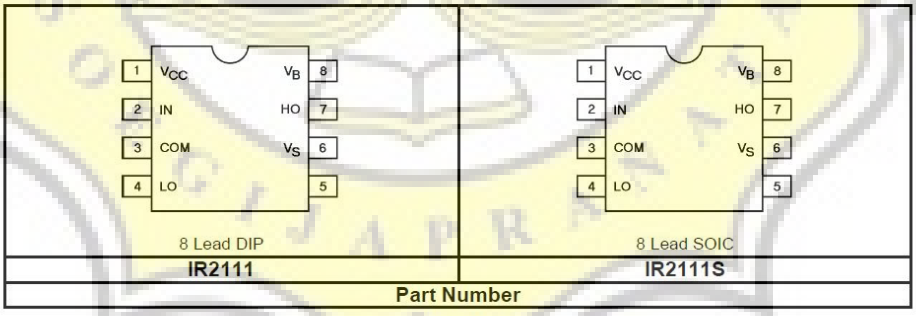
Functional Block Diagram



Lead Definitions

Symbol	Description
IN	Logic input for high side and low side gate driver outputs (HO & LO), in phase with HO
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
V_{CC}	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments



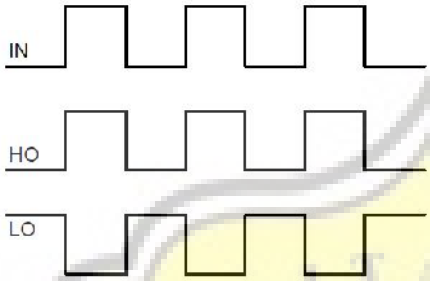


Figure 1. Input/Output Timing Diagram

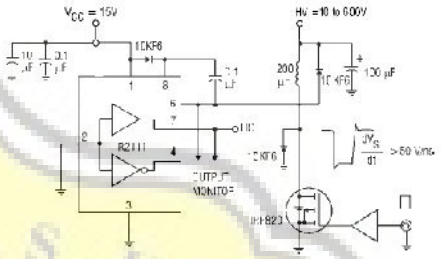


Figure 2. Floating Supply Voltage Transient Test Circuit

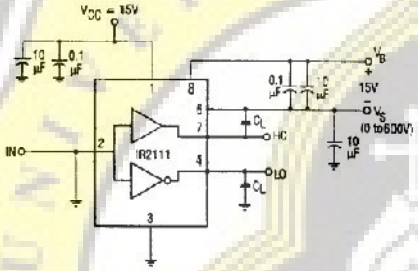


Figure 3. Switching Time Test Circuit

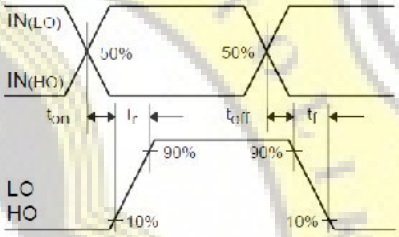


Figure 4. Switching Time Waveform Definition

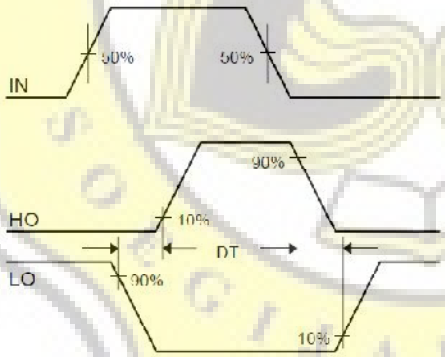


Figure 5. Deadtime Waveform Definitions

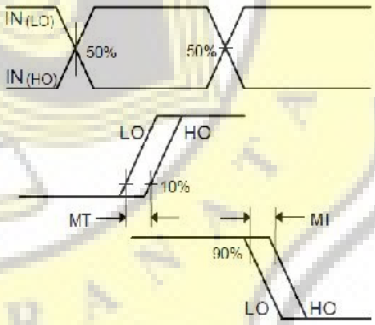


Figure 6. Delay Matching Waveform Definitions

Data sheet IR460

FAIRCHILD SEMICONDUCTOR®

IRFP460

Data Sheet | **January 2002**

20A, 500V, 0.270 Ohm, N-Channel Power MOSFET

This N-Channel enhancement mode silicon gate power field effect transistor is an advanced power MOSFET designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA17465.

Ordering Information

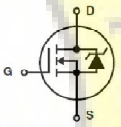
PART NUMBER	PACKAGE	BRAND
IRFP460	TO-247	IRFP460

NOTE: When ordering, use the entire part number.

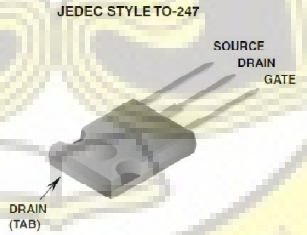
Features

- 20A, 500V
- $r_{DS(ON)} = 0.270\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Related Literature
  - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol



Packaging



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		IRFP460	UNITS
Drain to Source Voltage (Note 1)	V_{DS}	500	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	500	V
Continuous Drain Current	I_D	20	A
$T_C = 100^oC$	I_D	12	A
Pulsed Drain Current (Note 3)	I_{DM}	80	A
Gate to Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation	P_D	250	W
Linear Derating Factor		2.0	$W/^oC$
Single Pulse Avalanche Energy Rating (Note 4)	E_{AS}	960	mJ
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

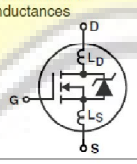
NOTE:

1. $T_J = 25^oC$ to $T_J = 125^oC$.

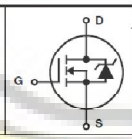
Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250µA, V_{GS} = 0V (Figure 10)	500	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250µA	2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, V_{GS} = 0V	-	-	25	µA
		V_{DS} = 0.8 x Rated BV_{DSS}, V_{GS} = 0V, $T_J = 125^oC$	-	-	250	µA
On-State Drain Current (Note 2)	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}$, V_{GS} = 10V	20	-	-	A
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V	-	-	±100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	I_D = 11A, V_{GS} = 10V (Figures 8, 9)	-	0.24	0.27	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq 50V$, $I_{DS} > 11A$ (Figure 12)	13	19	-	S
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 250V, I_D = 21A, R_{GS} = 4.3Ω, R_D = 12Ω, V_{GS} = 10V MOSFET Switching Times are Essentially Independent of Operating Temperature	-	23	35	ns
Rise Time	t_r		-	81	120	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	85	130	ns
Fall Time	t_f		-	65	98	ns
Total Gate Charge (Gate to Source + Gate-Drain)	$Q_{g(TOT)}$	V_{GS} = 10V, I_D = 21A, V_{DS} = 0.8 x Rated BV_{DSS}, $I_{G(REF)}$ = 1.5mA (Figure 14). Gate Charge is Essentially Independent of OperatingTemperature	-	120	190	nC
Gate to Source Charge	Q_{gs}		-	18	-	nC
Gate to Drain "Miller" Charge	Q_{gd}		-	62	-	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz (Figure 10)	-	4100	-	pF
Output Capacitance	C_{OSS}		-	480	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	84	-	pF
Internal Drain Inductance	L_D	Measured from the Drain Lead, 6mm (0.25in) from Package to Center of Die	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the Source Lead, 6mm (0.25in) from Header to Source Bonding Pad	-	13	-	nH
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	0.50	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Free Air Operation	-	-	30	$^oC/W$

Modified MOSFET Symbol Showing the Internal Device Inductances



Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I_{SD}	Modified MOSFET Symbol Showing the Integral Reverse P.N Junction Rectifier 	-	-	20	A
Pulse Source to Drain Current (Note 3)	I_{SDM}		-	-	80	A
Source to Drain Diode Voltage (Note 2)	V_{SD}	$T_J = 25^oC$, $I_{SD} = 21A$, $V_{GS} = 0V$ (Figure 13)	-	-	1.8	V
Reverse Recovery Time	t_{rr}	$T_J = 25^oC$, $I_{SD} = 21A$, $dI_{SD}/dt = 100A/\mu s$	280	580	1200	ns
Reverse Recovery Charge	Q_{RR}	$T_J = 25^oC$, $I_{SD} = 21A$, $dI_{SD}/dt = 100A/\mu s$	3.6	8.1	18	µC

NOTES:

2. Pulse test: pulse width ≤ 300µs, duty cycle ≤ 2%.
3. Repetitive rating: pulse width limited by Max junction temperature. See Transient Thermal Impedance curve (Figure 3).
4. $V_{DD} = 50V$, starting $T_J = 25^oC$, $L = 4.3mH$, $R_{GS} = 25\Omega$, Peak $I_{AS} = 20A$.

Typical Performance Curves Unless Otherwise Specified

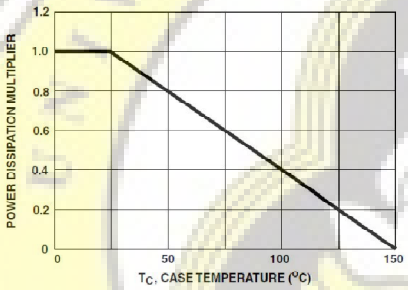


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

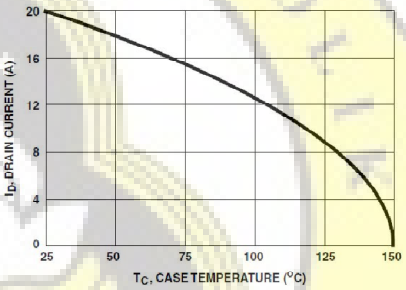


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

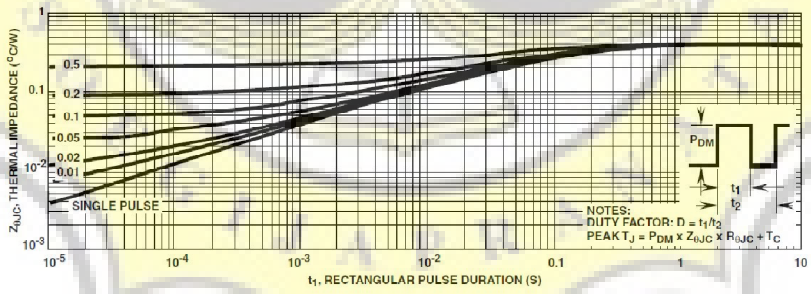


FIGURE 3. MAXIMUM TRANSIENT THERMAL IMPEDANCE

Typical Performance Curves Unless Otherwise Specified (Continued)

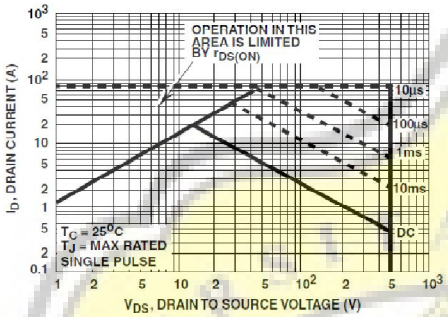


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

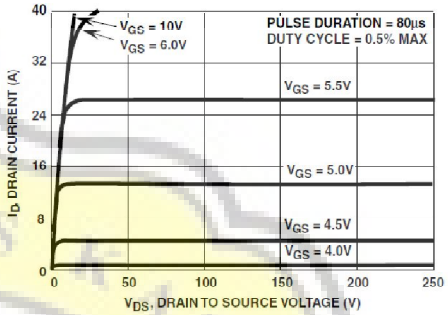


FIGURE 5. OUTPUT CHARACTERISTICS

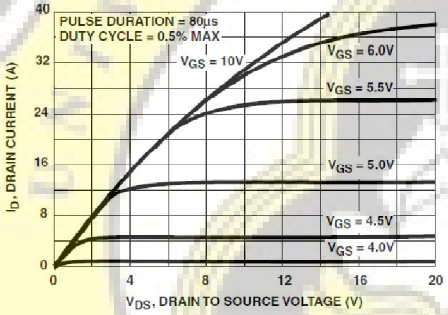


FIGURE 6. SATURATION CHARACTERISTICS

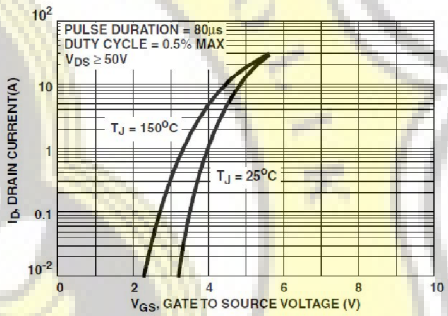


FIGURE 7. TRANSFER CHARACTERISTICS

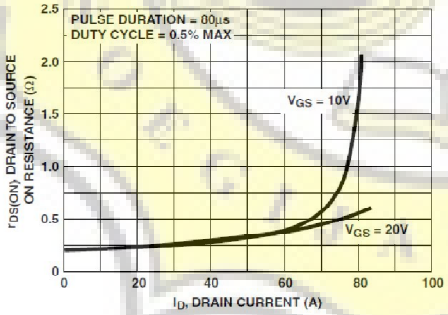


FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

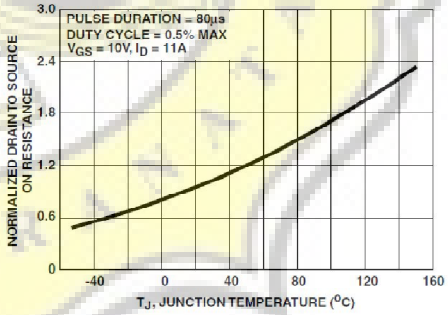


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Test Circuits and Waveforms

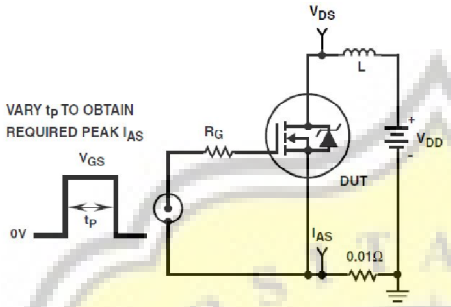


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

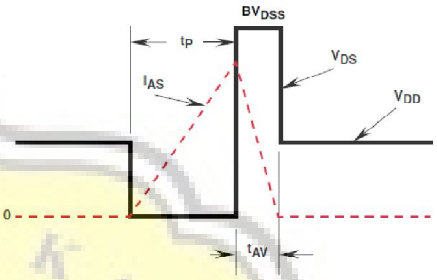


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

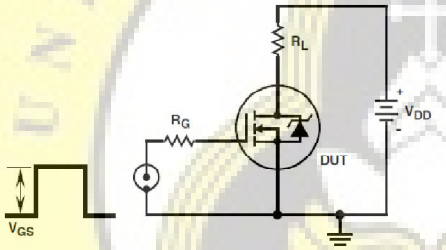


FIGURE 17. SWITCHING TIME TEST CIRCUIT

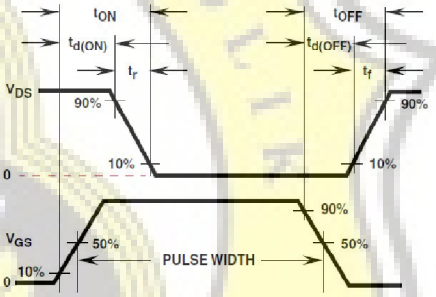


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

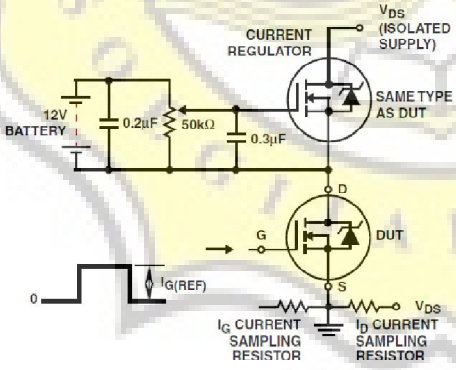


FIGURE 19. GATE CHARGE TEST CIRCUIT

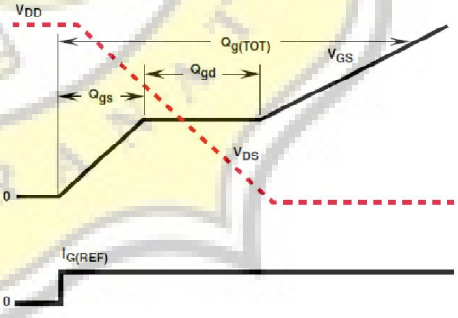


FIGURE 20. GATE CHARGE WAVEFORMS

Data sheet LM324

LM324, LM324A, LM224, LM2902, LM2902V, NCV2902

Single Supply Quad Operational Amplifiers

The LM324 series are low−cost, quad operational amplifiers with true differential inputs. They have several distinct advantages over standard operational amplifier types in single supply applications. The quad amplifier can operate at supply voltages as low as 3.0 V or as high as 32 V with quiescent currents about one−fifth of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

Features

- Short Circuited Protected Outputs
- True Differential Input Stage
- Single Supply Operation: 3.0 V to 32 V
- Low Input Bias Currents: 100 nA Maximum (LM324A)
- Four Amplifiers Per Package
- Internally Compensated
- Common Mode Range Extends to Negative Supply
- Industry Standard Pinouts
- ESD Clamps on the Inputs Increase Ruggedness without Affecting Device Operation
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

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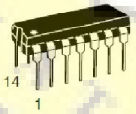
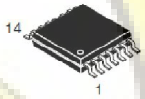


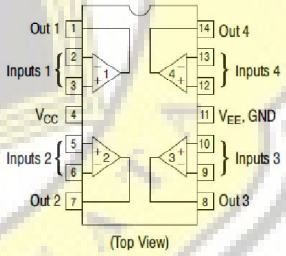
PDIP−14
N SUFFIX
CASE 646

SOIC−14
D SUFFIX
CASE 751A



TSSOP−14
DTB SUFFIX
CASE 948G

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 11 of this data sheet.

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages Single Supply Split Supplies	 V_{CC} V_{CC}, V_{EE}	 32 ±16	Vdc
Input Differential Voltage Range (Note 1)	V_{IDR}	±32	Vdc
Input Common Mode Voltage Range (Note 2)	V_{ICR}	−0.3 to 32	Vdc
Output Short Circuit Duration	t_{SC}	Continuous	
Junction Temperature	T_J	150	°C
Thermal Resistance, Junction−to−Air (Note 3) Case 646 Case 751A Case 948G	$R_{\theta JA}$	118 156 190	°C/W
Storage Temperature Range	T_{stg}	−65 to +150	°C
ESD Protection at any Pin Human Body Model Machine Model	V_{esd}	 2000 200	V
Operating Ambient Temperature Range LM224 LM324, 324A LM2902 LM2902V, NCV2902 (Note 4)	T_A	 −25 to +85 0 to +70 −40 to +105 −40 to +125	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Split Power Supplies.
2. For supply voltages less than 32 V, the absolute maximum input voltage is equal to the supply voltage.
3. All $R_{\theta JA}$ measurements made on evaluation board with 1 oz. copper traces of minimum pad size. All device outputs were active.
4. *NCV2902 is qualified for automitive use.*

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = GND, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	LM224			LM324A			LM324			LM2902			LM2902V/NCV2902			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage V_{CC} = 5.0 V to 30 V V_{ICR} = 0 V to V_{CC} −1.7 V, V_O = 1.4 V, R_S = 0 Ω	V_{IO}																mV
T_A = 25°C		–	2.0	5.0	–	2.0	3.0	–	2.0	7.0	–	2.0	7.0	–	2.0	7.0	
T_A = T_{high} (Note 5)		–	–	7.0	–	–	5.0	–	–	9.0	–	–	10	–	–	13	
T_A = T_{low} (Note 5)		–	–	7.0	–	–	5.0	–	–	9.0	–	–	10	–	–	10	
Average Temperature Coefficient of Input Offset Voltage T_A = T_{high} to T_{low} (Notes 5 and 7)	$\Delta V_{IO}/\Delta T$	–	7.0	–	–	7.0	30	–	7.0	–	–	7.0	–	–	7.0	–	μV/°C
Input Offset Current T_A = T_{high} to T_{low} (Note 5)	I_{IO}	– –	3.0 –	30 100	– –	5.0 –	30 75	– –	5.0 –	50 150	– –	5.0 –	50 200	– –	5.0 –	50 200	nA
Average Temperature Coefficient of Input Offset Current T_A = T_{high} to T_{low} (Notes 5 and 7)	$\Delta I_{IO}/\Delta T$	–	10	–	–	10	300	–	10	–	–	10	–	–	10	–	pA/°C
Input Bias Current T_A = T_{high} to T_{low} (Note 5)	I_{IB}	– –	–90 –	–150 –300	– –	–45 –	–100 –200	– –	–90 –	–250 –500	– –	–90 –	–250 –500	– –	–90 –	–250 –500	nA
Input Common Mode Voltage Range (Note 6) V_{CC} = 30 V	V_{ICR}																V
T_A = +25°C		0	–	28.3	0	–	28.3	0	–	28.3	0	–	28.3	0	–	28.3	
T_A = T_{high} to T_{low} (Note 5)		0	–	28	0	–	28	0	–	28	0	–	28	0	–	28	
Differential Input Voltage Range	V_{IDR}	–	–	V_{CC}	–	–	V_{CC}	–	–	V_{CC}	–	–	V_{CC}	–	–	V_{CC}	V
Large Signal Open Loop Voltage Gain R_L = 2.0 kΩ, V_{CC} = 15 V, for Large V_O Swing	A_{VOL}	50	100	–	25	100	–	25	100	–	25	100	–	25	100	–	V/mV
T_A = T_{high} to T_{low} (Note 5)		25	–	–	15	–	–	15	–	–	15	–	–	15	–	–	
Channel Separation 10 kHz ≤ f ≤ 20 kHz, Input Referenced	CS	–	–120	–	–	–120	–	–	–120	–	–	–120	–	–	–120	–	dB
Common Mode Rejection, R_S ≤ 10 kΩ	CMR	70	85	–	65	70	–	65	70	–	50	70	–	50	70	–	dB
Power Supply Rejection	PSR	65	100	–	65	100	–	65	100	–	50	100	–	50	100	–	dB

5. LM224: T_{low} = −25°C, T_{high} = +85°C
   LM324/LM324A: T_{low} = 0°C, T_{high} = +70°C
   LM2902: T_{low} = −40°C, T_{high} = +105°C
   LM2902V & NCV2902: T_{low} = −40°C, T_{high} = +125°C
   NCV2902 is qualified for automotive use.
6. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common mode voltage range is V_{CC} −1.7 V, but either or both inputs can go to +32 V without damage, independent of the magnitude of V_{CC}.
7. Guaranteed by design.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = GND, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	LM224			LM324A			LM324			LM2902			LM2902V/NCV2902			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage – High Limit	V_{OH}																V
V_{CC} = 5.0 V, R_L = 2.0 kΩ, T_A = 25°C		3.3	3.5	–	3.3	3.5	–	3.3	3.5	–	3.3	3.5	–	3.3	3.5	–	
V_{CC} = 30 V R_L = 2.0 kΩ (T_A = T_{high} to T_{low}) (Note 8)		26	–	–	26	–	–	26	–	–	26	–	–	26	–	–	
V_{CC} = 30 V R_L = 10 kΩ (T_A = T_{high} to T_{low}) (Note 8)		27	28	–	27	28	–	27	28	–	27	28	–	27	28	–	
Output Voltage – Low Limit, V_{CC} = 5.0 V, R_L = 10 kΩ, T_A = T_{high} to T_{low} (Note 8)	V_{OL}	–	5.0	20	–	5.0	20	–	5.0	20	–	5.0	100	–	5.0	100	mV
Output Source Current (V_{ID} = +1.0 V, V_{CC} = 15 V)	I_{O+}																mA
T_A = 25°C		20	40	–	20	40	–	20	40	–	20	40	–	20	40	–	
T_A = T_{high} to T_{low} (Note 8)		10	20	–	10	20	–	10	20	–	10	20	–	10	20	–	
Output Sink Current	I_{O-}																mA
(V_{ID} = –1.0 V, V_{CC} = 15 V) T_A = 25°C		10	20	–	10	20	–	10	20	–	10	20	–	10	20	–	
T_A = T_{high} to T_{low} (Note 8)		5.0	8.0	–	5.0	8.0	–	5.0	8.0	–	5.0	8.0	–	5.0	8.0	–	
(V_{ID} = –1.0 V, V_O = 200 mV, T_A = 25°C)		12	50	–	12	50	–	12	50	–	–	–	–	–	–	–	µA
Output Short Circuit to Ground (Note 9)	I_{SC}	–	40	60	–	40	60	–	40	60	–	40	60	–	40	60	mA
Power Supply Current (T_A = T_{high} to T_{low}) (Note 8)	I_{CC}																mA
V_{CC} = 30 V V_O = 0 V, R_L = ∞		–	–	3.0	–	1.4	3.0	–	–	3.0	–	–	3.0	–	–	3.0	
V_{CC} = 5.0 V, V_O = 0 V, R_L = ∞		–	–	1.2	–	0.7	1.2	–	–	1.2	–	–	1.2	–	–	1.2	

8. LM224: T_{low} = –25°C, T_{high} = +85°C
LM324/LM324A: T_{low} = 0°C, T_{high} = +70°C
LM2902: T_{low} = –40°C, T_{high} = +105°C
LM2902V & NCV2902: T_{low} = –40°C, T_{high} = +125°C
NCV2902 is qualified for automotive use.
9. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common mode voltage range is V_{CC} –1.7 V, but either or both inputs can go to +32 V without damage, independent of the magnitude of V_{CC}.

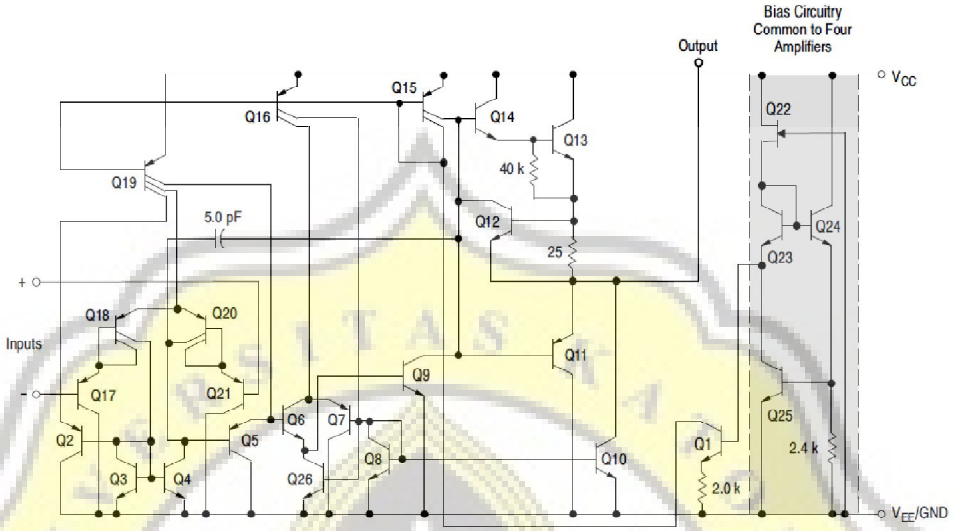


Figure 1. Representative Circuit Diagram
(One−Fourth of Circuit Shown)

Mikrokontrol *dsPIC30F4012*

MICROCHIP

dsPIC30F4011/4012

dsPIC30F4011/4012 Enhanced Flash 16-bit Digital Signal Controller

Note: This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the *dsPIC30F Family Reference Manual* (DS70046). For more information on the device instruction set and programming, refer to the *dsPIC30F Programmer's Reference Manual* (DS70030).

High Performance Modified RISC CPU:

- Modified Harvard architecture
- C compiler optimized instruction set architecture with flexible addressing modes
- 84 base instructions
- 24-bit wide instructions, 16-bit wide data path
- 48 Kbytes on-chip Flash program space (16K Instruction words)
- 2 Kbytes of on-chip data RAM
- 1 Kbytes of non-volatile data EEPROM
- Up to 30 MIPs operation:
  - DC to 40 MHz external clock input
  - 4 MHz-10 MHz oscillator input with PLL active (4x, 8x, 16x)
- 30 interrupt sources
  - 3 external interrupt sources
  - 8 user selectable priority levels for each interrupt source
  - 4 processor trap sources
- 16 x 16-bit working register array

DSP Engine Features:

- Dual data fetch
- Accumulator write back for DSP operations
- Modulo and Bit-Reversed Addressing modes
- Two, 40-bit wide accumulators with optional saturation logic
- 17-bit x 17-bit single cycle hardware fractional/ integer multiplier
- All DSP instructions single cycle
- ± 16-bit single cycle shift

Peripheral Features:

- High current sink/source I/O pins: 25 mA/25 mA
- Timer module with programmable prescaler:
  - Five 16-bit timers/counters; optionally pair 16-bit timers into 32-bit timer modules
- 16-bit Capture input functions
- 16-bit Compare/PWM output functions
- 3-wire SPI™ modules (supports 4 Frame modes)
- I^2C™ module supports Multi-Master/Slave mode and 7-bit/10-bit addressing
- 2 UART modules with FIFO Buffers
- 1 CAN modules, 2.0B compliant

Motor Control PWM Module Features:

- 6 PWM output channels
  - Complementary or Independent Output modes
  - Edge and Center Aligned modes
- 3 duty cycle generators
- Dedicated time base
- Programmable output polarity
- Dead-time control for Complementary mode
- Manual output control
- Trigger for A/D conversions

Quadrature Encoder Interface Module Features:

- Phase A, Phase B and Index Pulse input
- 16-bit up/down position counter
- Count direction status
- Position Measurement (x2 and x4) mode
- Programmable digital noise filters on inputs
- Alternate 16-bit Timer/Counter mode
- Interrupt on position counter rollover/underflow

dsPIC30F4011/4012

Analog Features:

- 10-bit Analog-to-Digital Converter (A/D) with 4 S/H Inputs:
  - 500 Ksps conversion rate
  - 9 input channels
  - Conversion available during Sleep and Idle
- Programmable Brown-out Detection and Reset generation

Special Microcontroller Features:

- Enhanced Flash program memory:
  - 10,000 erase/write cycle (min.) for industrial temperature range, 100K (typical)
- Data EEPROM memory:
  - 100,000 erase/write cycle (min.) for industrial temperature range, 1M (typical)
- Self-reprogrammable under software control
- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Flexible Watchdog Timer (WDT) with on-chip low power RC oscillator for reliable operation
- Fail-Safe clock monitor operation detects clock failure and switches to on-chip low power RC oscillator
- Programmable code protection
- In-Circuit Serial Programming™ (ICSP™)
- Selectable Power Management modes
  - Sleep, Idle and Alternate Clock modes

CMOS Technology:

- Low power, high speed Flash technology
- Wide operating voltage range (2.5V to 5.5V)
- Industrial and Extended temperature ranges
- Low power consumption

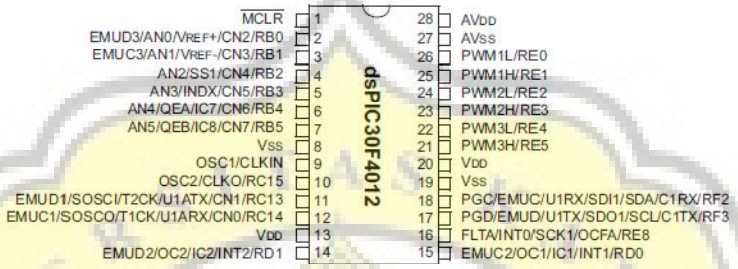
dsPIC30F Motor Control and Power Conversion Family*

Device	Pins	Program Mem. Bytes/ Instructions	SRAM Bytes	EEPROM Bytes	Timer 16-bit	Input Cap	Output Comp/Std PWM	Moto Control PWM	A/D 10-bit 500 Ksps	Quad Enc	UART	SPI™	I²C™	CAN
dsPIC30F2010	28	12K/4K	512	1024	3	4	2	6 ch	6 ch	Yes	1	1	1	-
dsPIC30F3010	28	24K/8K	1024	1024	5	4	2	6 ch	6 ch	Yes	1	1	1	-
dsPIC30F4012	28	48K/16K	2048	1024	5	4	2	6 ch	6 ch	Yes	1	1	1	1
dsPIC30F3011	40/44	24K/8K	1024	1024	5	4	4	6 ch	9 ch	Yes	2	1	1	-
dsPIC30F4011	40/44	48K/16K	2048	1024	5	4	4	6 ch	9 ch	Yes	2	1	1	1
dsPIC30F5015	64	66K/22K	2048	1024	5	4	4	8 ch	16 ch	Yes	1	2	1	1
dsPIC30F6010	80	144K/48K	8192	4096	5	8	8	8 ch	16 ch	Yes	2	2	1	2

* This table provides a summary of the dsPIC30F6010 peripheral features. Other available devices in the dsPIC30F Motor Control and Power Conversion Family are shown for feature comparison.

Pin Diagrams (Continued)

28-Pin SPDIP
28-Pin SOIC



44-Pin QFN

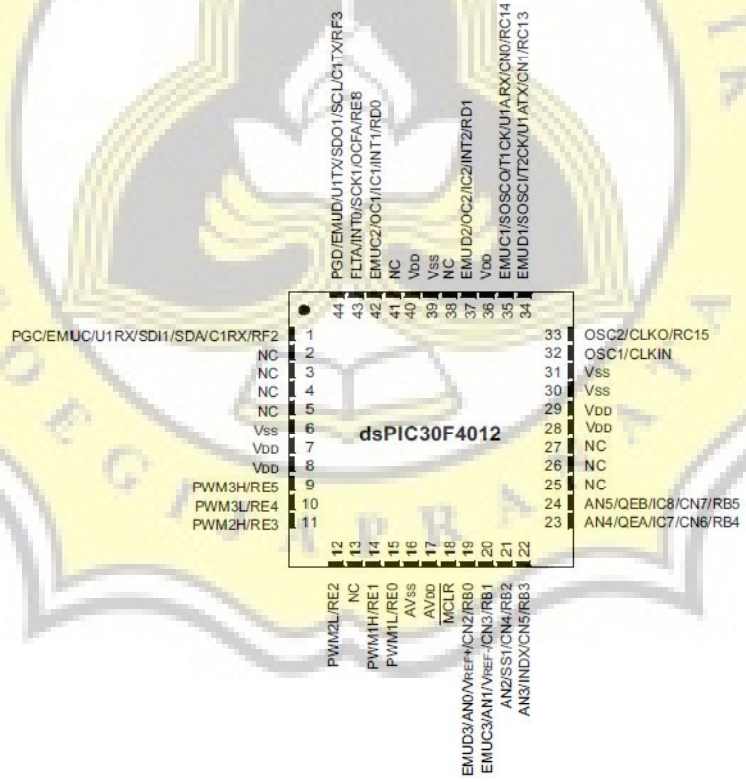


FIGURE 1-2: dsPIC30F4012 BLOCK DIAGRAM

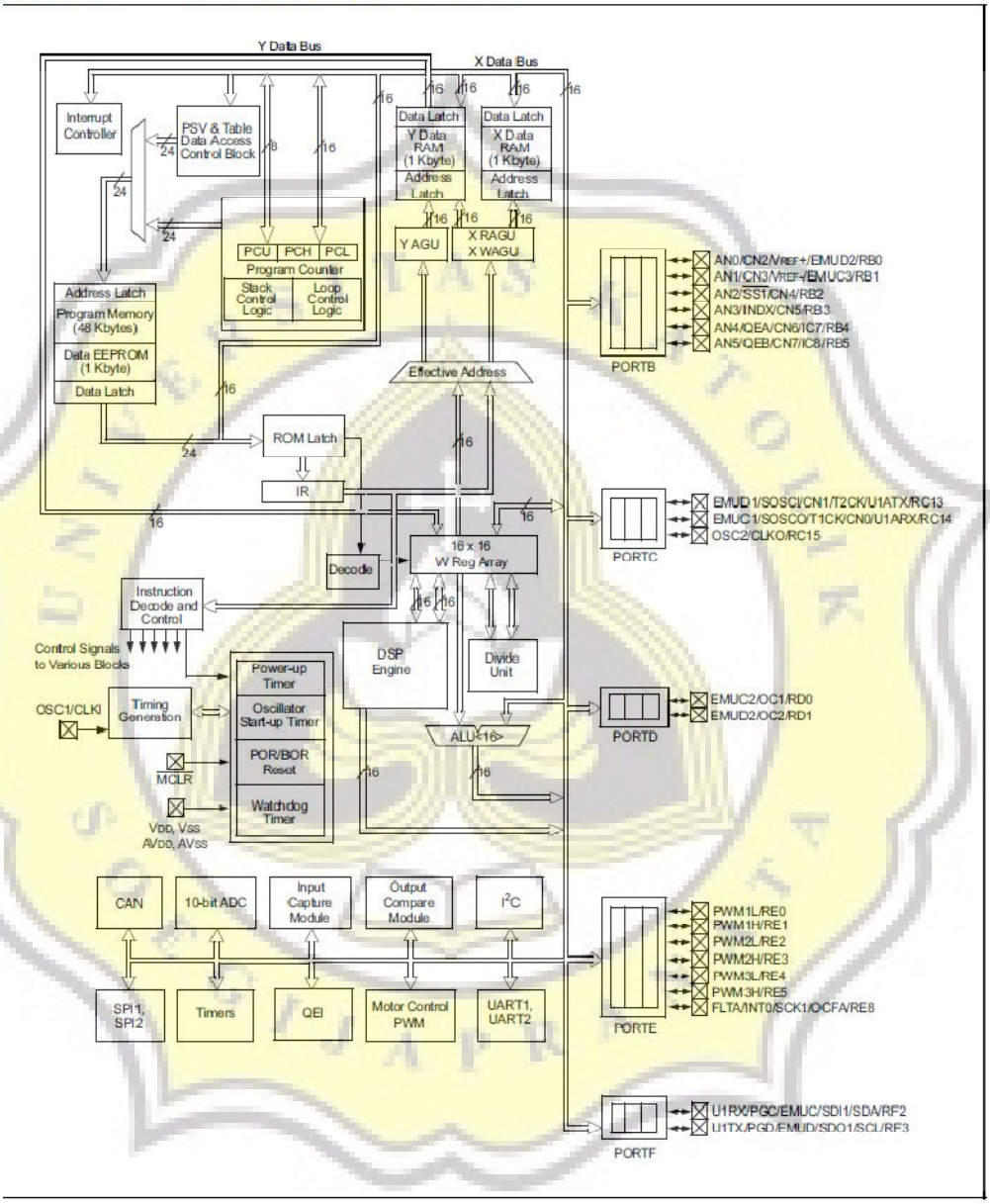


Table 1-2 provides a brief description of the device I/O pinout and the functions that are multiplexed to a port pin. Multiple functions may exist on one port pin. When multiplexing occurs, the peripheral module's functional requirements may force an override of the data direction of the port pin.

TABLE 1-2: dsPIC30F4012 I/O PIN DESCRIPTIONS

Pin Name	Pin Type	Buffer Type	Description
AN0-AN5	I	Analog	Analog input channels. AN0 and AN1 are also used for device programming data and clock inputs, respectively.
AVDD	P	P	Positive supply for analog module.
AVSS	P	P	Ground reference for analog module.
CLKI CLKO	I O	ST/CMOS —	External clock source input. Always associated with OSC1 pin function. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
CN0-CN7	I	ST	Input change notification inputs. Can be software programmed for internal weak pull-ups on all inputs.
C1RX C1TX	I O	ST —	CAN1 bus receive pin. CAN1 bus transmit pin.
EMUD EMUC EMUD1 EMUC1 EMUD2 EMUC2 EMUD3 EMUC3	I/O I/O I/O I/O I/O I/O I/O I/O	ST ST ST ST ST ST ST ST	ICD Primary Communication Channel data input/output pin. ICD Primary Communication Channel clock input/output pin. ICD Secondary Communication Channel data input/output pin. ICD Secondary Communication Channel clock input/output pin. ICD Tertiary Communication Channel data input/output pin. ICD Tertiary Communication Channel clock input/output pin. ICD Quaternary Communication Channel data input/output pin. ICD Quaternary Communication Channel clock input/output pin.
IC1, IC2, IC7, IC8	I	ST	Capture inputs 1, 2, 7 and 8.
INDX QEA QEB	I I I	ST ST ST	Quadrature Encoder Index Pulse input. Quadrature Encoder Phase A input in QEI mode. Auxiliary Timer External Clock/Gate input in Timer mode. Quadrature Encoder Phase A input in QEI mode. Auxiliary Timer External Clock/Gate input in Timer mode.
INT0 INT1 INT2	I I I	ST ST ST	External interrupt 0. External interrupt 1. External interrupt 2.
FLTA PWM1L PWM1H PWM2L PWM2H PWM3L PWM3H	I O O O O O O	ST — — — — — —	PWM Fault A input. PWM 1 Low output. PWM 1 High output. PWM 2 Low output. PWM 2 High output. PWM 3 Low output. PWM 3 High output.
MCLR	I/P	ST	Master Clear (Reset) input or programming voltage input. This pin is an active low Reset to the device.
OCFA OC1, OC2	I O	ST —	Compare Fault A input (for Compare channels 1, 2, 3 and 4). Compare outputs 1 and 2.

Legend: CMOS = CMOS compatible input or output; Analog = Analog input
ST = Schmitt Trigger input with CMOS levels; O = Output
I = Input; P = Power

TABLE 1-2: dsPIC30F4012 I/O PIN DESCRIPTIONS (CONTINUED)

Pin Name	Pin Type	Buffer Type	Description
OSC1 OSC2	I I/O	ST/CMOS —	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
PGD PGC	I/O I	ST ST	In-Circuit Serial Programming data input/output pin. In-Circuit Serial Programming clock input pin.
RB0-RB5	I/O	ST	PORTB is a bidirectional I/O port.
RC13-RC15	8I/O	8ST	PORTC is a bidirectional I/O port.
RD0-RD1	I/O	ST	PORTD is a bidirectional I/O port.
RE0-RE5, RE8	I/O	ST	PORTE is a bidirectional I/O port.
RF2-RF3	I/O	ST	PORTF is a bidirectional I/O port.
SCK1 SDI1 SDO1	I/O I O	ST ST —	Synchronous serial clock input/output for SPI1. SPI1 Data In. SPI1 Data Out.
SCL SDA	I/O I/O	ST ST	Synchronous serial clock input/output for I^2C. Synchronous serial data input/output for I^2C.
SOSCO SOSCI	O I	— ST/CMOS	32 kHz low power oscillator crystal output. 32 kHz low power oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
T1CK T2CK	I I	ST ST	Timer1 external clock input. Timer2 external clock input.
U1RX U1TX U1ARX U1ATX	I O I O	ST — ST —	UART1 Receive. UART1 Transmit. UART1 Alternate Receive. UART1 Alternate Transmit.
VDD	P	—	Positive supply for logic and I/O pins.
VSS	P	—	Ground reference for logic and I/O pins.
VREF+	I	Analog	Analog Voltage Reference (High) input.
VREF-	I	Analog	Analog Voltage Reference (Low) input.

Legend: CMOS = CMOS compatible input or output Analog = Analog Input
ST = Schmitt Trigger input with CMOS levels O = Output
I = Input P = Power