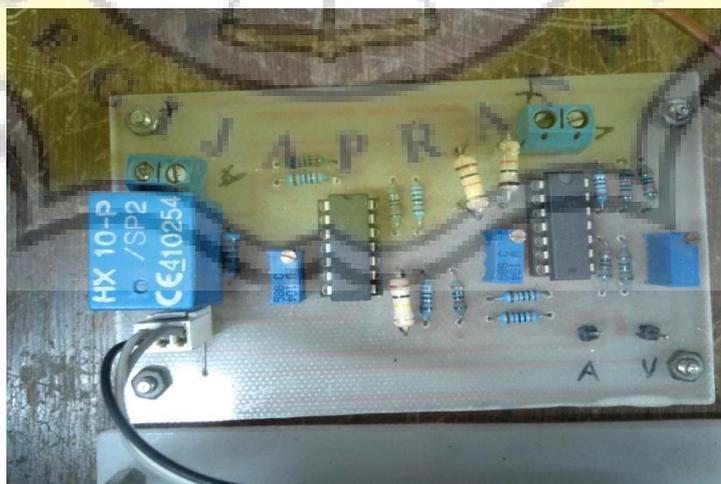
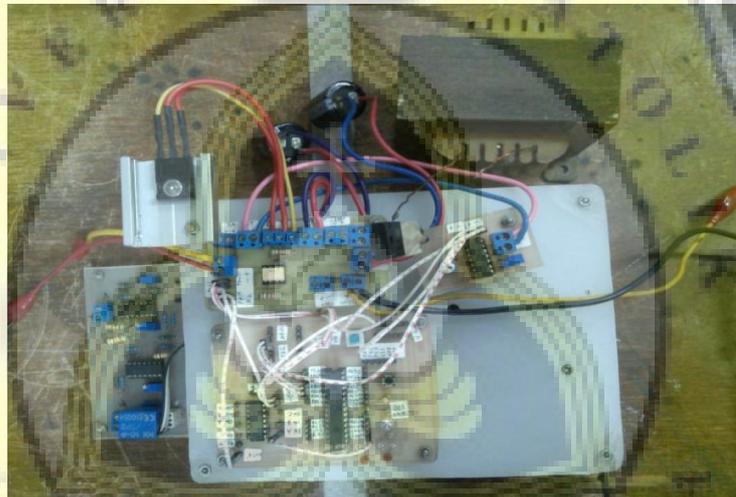
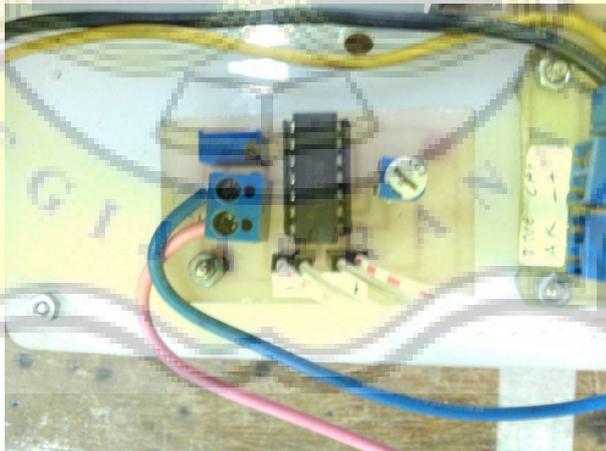
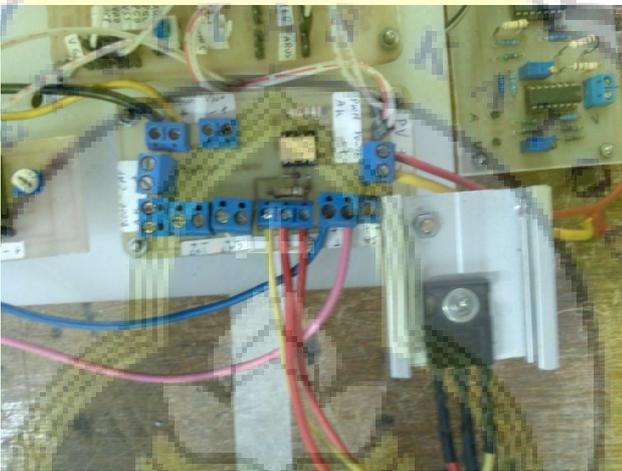
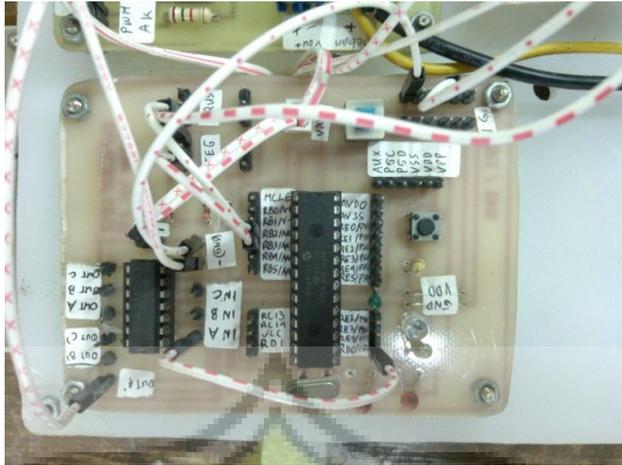


LAMPIRAN





TLP250

- Transistor Inverter
- Inverter For Air Conditionor
- IGBT Gate Drive
- Power MOS FET Gate Drive

The TOSHIBA TLP250 consists of a GaAlAs light emitting diode and a integrated photodetector.

This unit is 8-lead DIP package.

TLP250 is suitable for gate driving circuit of IGBT or power MOS FET.

- Input threshold current: $I_F=5\text{mA}(\text{max.})$
- Supply current (I_{CC}): $11\text{mA}(\text{max.})$
- Supply voltage (V_{CC}): $10\text{--}35\text{V}$
- Output current (I_O): $\pm 1.5\text{A}(\text{max.})$
- Switching time (t_{pLH}/t_{pHL}): $1.5\mu\text{s}(\text{max.})$
- Isolation voltage: $2500\text{V}_{\text{rms}}(\text{min.})$
- UL recognized: UL1577, file No.E67349

• Option (D4) type

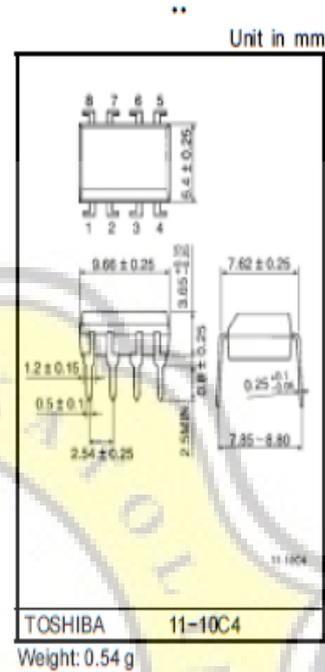
VDE approved: DIN VDE0884/06.92,certificate No.76823

Maximum operating insulation voltage: 630V_{PK}

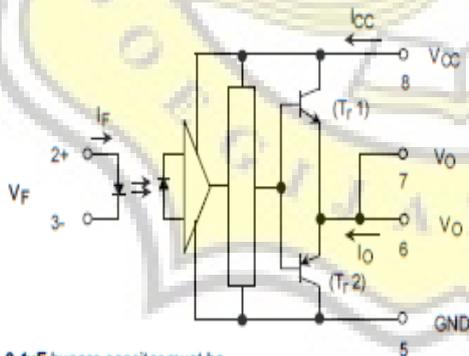
Highest permissible over voltage: 4000V_{PK}

(Note) When a VDE0884 approved type is needed, please designate the "option (D4)"

- Creepage distance: $6.4\text{mm}(\text{min.})$
- Clearance: $6.4\text{mm}(\text{min.})$

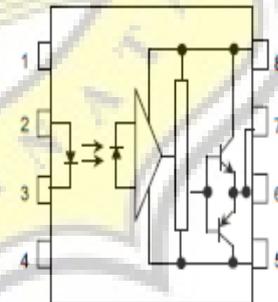


Schematic



A $0.1\mu\text{F}$ bypass capacitor must be connected between pin 8 and 5 (See Note 5).

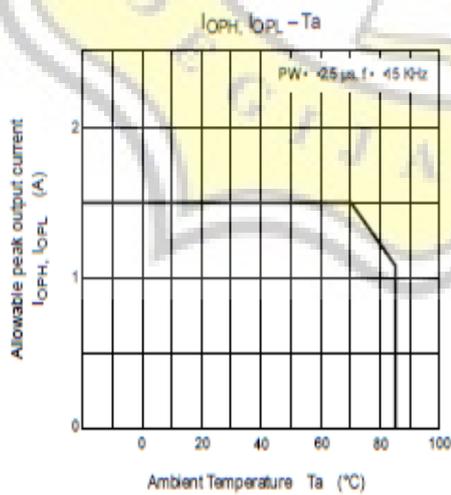
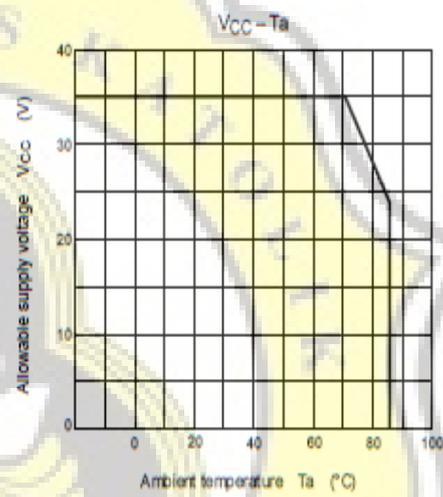
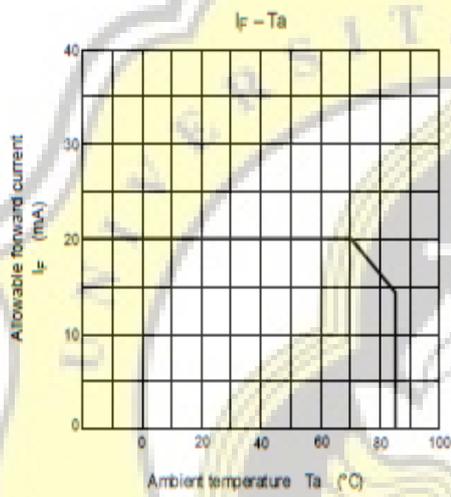
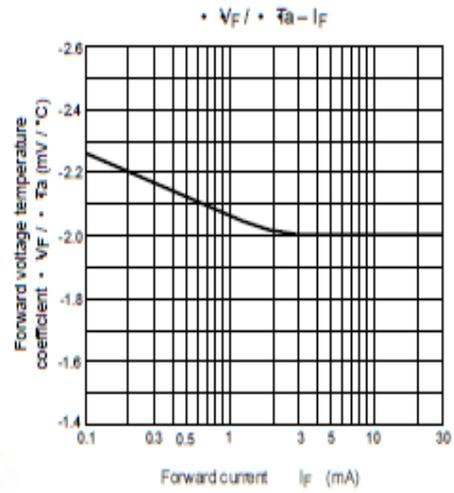
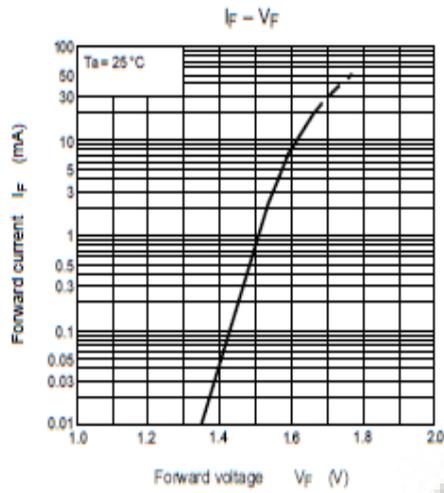
Pin Configuration (top view)



- 1 : N.C.
- 2 : Anode
- 3 : Cathode
- 4 : N.C.
- 5 : GND
- 6 : V_O (Output)
- 7 : V_O
- 8 : V_{CC}

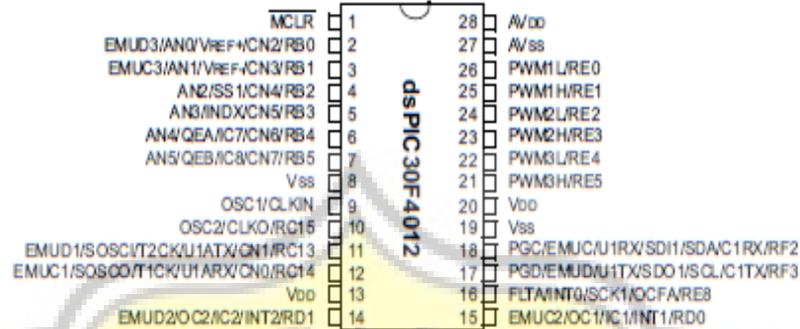
Truth Table

		Tr1	Tr2
Input LED	On	On	Off
	Off	Off	On



Pin Diagrams (Continued)

28-Pin SPDIP
28-Pin SOIC



44-Pin QFN

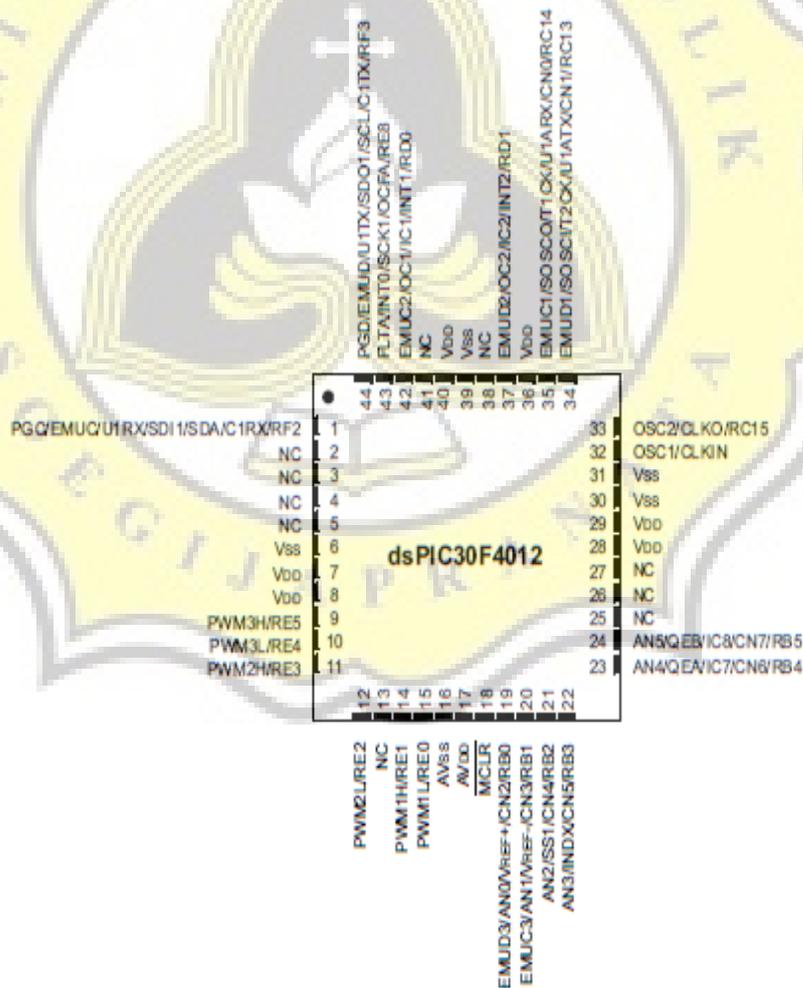
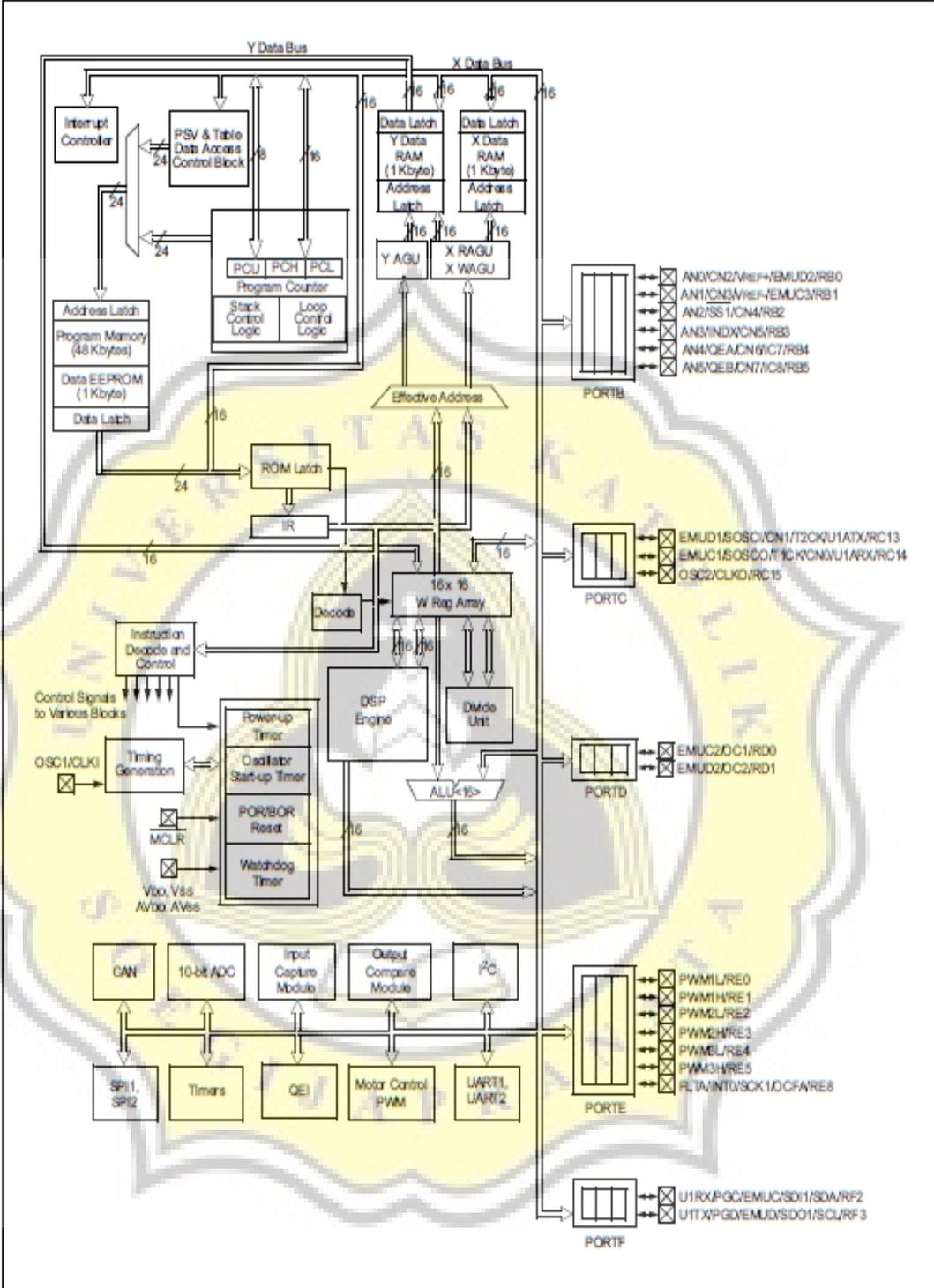


FIGURE 1-2: dsPIC30F4012 BLOCK DIAGRAM



/*

=====

KONTROL MPPT INCREMENTAL CONDUCTANCE (VOLTAGE CONTROL)

INPUT VOLTAGE = RB3

INPUT CURRENT = RB2

OUTPUT TO GATE = LATD

Test configuration MCU : dsPIC30F4012 (8 MHz)

=====

*/

unsigned char ADC2,ADC3,V,I;

signed int duty;

signed long dI,dV,lastI,lastV;

signed long Pembagi1,Pembagi2;

signed long hasil1,hasil2,tambah;

signed long Error,kurang;

void Timer1Int() iv IVT_ADDR_T1INTERRUPT

{

T1IF_bit = 0; // Clear T1IF

ADCON1bits.SAMP = 1;

IFS0bits.ADIF = 0; // clear interrupt

while (IFS0bits.ADIF); // conversion done?

{

ADC2 = ADCBUF0;

ADC3 = ADCBUF1;

}

I = ADC2;

V = ADC3;

lastI = I;

lastV = V;

dI = I - lastI;

```

dV = V - lastV;

Pembagi1=dI/dV;

Pembagi2=hasil1/Pembagi1;

hasil1=I*(-1);

hasil2=V*(-1);

tambah=Pembagi2+hasil2;

Error=kurang;

if (Error > 25)
{
if (duty >= PR1)
duty = PR1-1;    //duty maksimum
else
duty++;
}
if (Error < 25)    //dP positif dI negatif
{
if (duty <= 3 )
duty = 4;    //duty minimum
else
duty--;
}
}

void main()
{
TRISD = 0;

LATD = 0;

lastI = 0;

lastV = 0;

duty = 50;

ADPCFG = 0xFFFF3;    // RB2 & RB3 = analog

```

```

ADCON1 = 0x00E0;           // SIMSAM bit = 0 : Samples multiple channels
                             // individually in sequence

                             // ASAM = 0 : Sampling begins when SAMP bit set

                             // SSRC = 111 auto-convert

ADCHS = 0x0302;           // Connect AN3 as CH0 input (MUXB) and AN2 as CH0
                             // (MUXA)

ADCSSL = 0;

ADCON3 = 0x0302;           // Auto Sampling 3 Tad, Tad = internal 2 Tcy

ADCON2 = 0x6005;           // Eksternal Vref
                             // only sample CH0
                             // SMPI = 0001 for interrupt after 2 converts
                             // MUXA and MUXB alternate

ADCON1bits.ADON = 1;      // turn ADC ON

IPC0 = IPC0 | 0x1000;      // Interrupt priority level = 1

T1IF_bit = 0;             // Clear T1IF

T1IE_bit = 1;             // Enable Timer1 interrupts

T1CON = 0x8000;           // Timer1 ON, internal clock FCY, prescaler

PR1 = 6000;               // L inti ferit (1500 s/d 2500 / L inti besi (6000) //1300

while (1)
{
    if (duty >= TMR1)
        LATD = 0xFFFF;
    else
        LATD = 0;
}
}

```

Cetak - Tutup Jendela - Klik Lebihnya pada bagian bawah email untuk mencetak pesan tunggal

Judul:	Hasil Review Paper IRWNS 2014
Dari:	Irwns - (irwns@polban.ac.id)
Kepada:	adi.kurniawan07@ymail.com; adilasosianika@yahoo.com; mardhatrimeilani@polban.ac.id;
Tanggal:	Minggu, 12 Oktober 2014 15:45

Kepada

Ysh. Bpk Adhi Kurniawan

Dengan senang hati kami informasikan bahwa paper Bapak **diterima** untuk dipresentasikan di Industrial Research Workshop and National Seminar (IRWNS) 2014 **dengan beberapa revisi didalamnya**. Untuk itu kami kirimkan hasil penilaian/revisi dari tim reviewer IRWNS, dan kami harapkan hasil revisinya dapat kami terima dalam kurun waktu **3 (tiga) hari sejak kami kirimkan**.

Selanjutnya kami megundang Bapak/ Ibu untuk hadir pada Rabu tanggal **12 November 2014 di Politeknik Negeri Bandung**.

Untuk proses selanjutnya, kami mohon Bapak/ Ibu dapat mengisi dan mengirimkan formulir terlampir kepada panitia IRWNS 2014 (email: **irwns@polban.ac.id**).

Hormat kami,

Panitia IRWNS 2014