NO :	Nama :	Data :												
		Hexadecimal	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11
1	Yohanes Catur R	156	0	1	1	0	1	0	1	0	1	0	0	0
	01.50.0116	135	1	0	1	0	1	1	0	0	1	0	0	0
		107	1	1	1	0	0	0	0	0	1	0	0	0
		115	1	0	1	0	1	0	0	0	1	0	0	0
		115	1	0	1	0	1	0	0	0	1	0	0	0
		125	1	0	1	0	0	1	0	0	1	0	0	0
		160	0	0	0	0	0	1	1	0	1	0	0	0
		187	1	1	1	0	0	0	0	1	1	0	0	0
		133	1	1	0	0	1	1	0	0	1	0	0	0
		135	1	0	1	0	1	1	0	0	1	0	0	0
2	Indro DS	090	0	0	0	0	0	1	0	1	0	0	0	0
	99.50.0386	0B4	0	1	0	0	1	0	0	1	0	0	0	0
		0B4	0	0	1	0	1	1	0	1	0	0	0	0
		0B4	0	0	1	0	1	1	0	1	0	0	0	0
		093	1	1	0	0	1	0	1	1	0	0	0	0
		0A6	0	1	1	0	0	1	0	1	0	0	0	0
		0F4	0	0	1	0	1	1	1	1	0	0	0	0
		090	0	0	0	0	1	0	0	1	0	0	0	0
		097	1	1	1	0	1	0	0	1	0	0	0	0
		0D4	0	0	1	0	1	0	1	1	0	0	0	0
3.	Danang	095	1	0	1	0	1	1	0	1	0	0	0	0
	Ristiawan	0E7	1	1	1	0	0	1	1	1	0	0	0	0
	02.81.0023	093	1	1	0	0	1	0	0	1	0	0	0	0
		093	1	1	0	0	0	0	0	1	0	0	0	0
		0A3	1	1	0	0	0	1	0	1	0	0	0	0
		095	1	0	1	0	1	0	0	1	0	0	0	0
		0A5	1	0	1	0	0	1	0	1	0	0	0	0
		051	1	0	0	0	1	0	1	0	0	0	0	0
		086	0	1	1	0	0	0	0	1	0	0	0	0
		0C4	0	0	1	0	0	1	0	1	0	0	0	0
4.	Andreas Andi S	143	1	1	0	0	0	0	1	0	1	0	0	0
	05.11.0045	106	0	1	1	0	0	0	0	0	1	0	0	0
		0F4	1	0	1	0	0	1	0	1	0	0	0	0
		0C4	1	1	0	0	1	1	1	1	0	0	0	0
		144	0	0	1	0	0	0	1	0	1	0	0	0
		0C0	0	0	0	0	0	1	0	1	0	0	0	0
		0F7	1	1	1	0	1	1	1	1	0	0	0	0
		141	1	0	0	0	0	0	1	0	1	0	0	0
		0D7	1	1	1	0	1	0	1	1	0	0	0	0
		0B2	0	1	0	0	1	1	0	1	0	0	0	0
5.	Danu Agung	141	1	0	0	0	0	0	1	0	1	0	0	0
	05.11.0026	160	0	0	0	0	0	1	1	0	1	0	0	0
		0C3	1	0	0	0	1	1	0	1	0	0	0	0
		293	1	1	0	0	1	0	0	1	0	1	0	0
		2F2	0	1	0	0	1	1	1	1	0	1	0	0
		293	1	1	0	0	1	0	0	1	0	1	0	0
		382	0	1	0	0	0	0	0	1	1	1	0	0

		212	0	1	0	0	1	0	0	0	0	1	0	0
		365	1	0	1	0	0	1	1	0	1	1	0	0
		286	0	1	1	0	1	1	0	1	0	1	0	0
6.	Sony Cristian	0C2	0	1	0	0	1	1	0	1	0	0	0	0
	02.60.0232	0CA	0	0	0	0	1	1	0	1	0	0	0	0
		0E7	0	1	0	1	0	1	1	0	0	0	0	0
		050	1	1	1	0	1	1	1	0	0	0	0	0
		092	0	0	0	0	1	0	1	0	0	0	0	0
		075	0	1	0	0	1	0	0	1	0	0	0	0
		030	1	0	1	0	1	1	1	0	0	0	0	0
		0E3	0	0	0	0	0	1	1	0	0	0	0	0
		030	0	0	0	0	1	1	1	0	0	0	0	0
		0E3	1	1	0	0	1	1	1	0	0	0	0	0
7.	Hermanto Pali		1	1	1	0	1	1	1	0	0	0	0	0
	02.80.0066	117	0	1	1	0	0	1	1	0	0	0	0	0
		112	1	1	1	0	1	0	0	0	1	0	0	0
		135	0	1	0	0	1	0	0	0	1	0	0	0
		116	1	0	1	0	1	1	0	0	1	0	0	0
		100	0	1	1	0	1	0	0	0	1	0	0	0
		166	0	0	0	0	0	0	0	0	1	0	0	0
		100	0	1	1	0	0	1	1	0	1	0	0	0
		166	1	1	1	0	0	1	0	0	1	0	0	0
		127	1	1	1	0	0	1	0	0	1	0	0	0
8.	Eric AP	070	0	0	0	0	1	1	1	0	0	0	0	0
	04.60.0206	047	1	1	0	0	0	0	1	0	0	0	0	0
		207	1	1	1	0	0	0	0	0	0	1	0	0
		097	1	1	1	0	1	0	0	1	0	0	0	0
		0B5	1	0	1	0	1	1	0	1	0	0	0	0
		0A5	1	0	1	0	0	1	0	1	0	0	0	0
		0D6	0	1	1	0	1	0	1	1	0	0	0	0
		0A6	0	1	1	0	0	1	0	1	0	0	0	0
		071	1	0	0	0	1	1	1	0	0	0	0	0
		084	0	0	1	0	0	0	0	1	0	0	0	0
9.	Agus S	073	1	1	0	0	1	1	1	0	0	0	0	0
	03.50.0061	063	1	1	0	0	0	1	1	0	0	0	0	0
		057	1	0	0	0	0	0	0	1	0	0	0	0
		182	1	1	1	0	1	0	1	0	0	0	0	0
		0A0	0	1	0	0	0	0	0	1	1	0	0	0
		090	0	0	0	0	0	1	0	1	0	0	0	0
		0B2	0	0	0	0	1	0	0	1	0	0	0	0
		023	0	1	0	0	1	1	0	1	0	0	0	0
		155	1	1	0	0	0	1	0	1	0	0	0	0
		115	1	0	1	0	1	0	1	0	1	0	0	0
10.	Vincent	133	1	1	0	0	1	1	0	0	1	0	0	0
	03.50.0016	105	1	0	1	0	0	0	0	0	1	0	0	0
		041	1	0	0	0	0	0	1	0	0	0	0	0
		074	0	0	1	0	1	1	1	1	0	0	0	0
		012	0	1	0	0	0	1	0	0	0	0	0	0
		0C6	0	1	1	0	1	1	0	1	0	0	0	0

		080	0	0	0	0	0	0	0	1	0	0	0	0
		083	1	1	0	0	0	0	0	1	0	0	0	0
		074	0	0	1	0	1	1	1	0	0	0	0	0
		217	1	1	1	0	1	0	0	0	0	1	0	0
11.	Hery W	1E0	0	0	0	0	0	1	1	1	1	0	0	0
		1C4	0	0	1	0	0	0	1	1	1	0	0	0
		1B4	0	0	1	0	1	1	0	1	1	0	0	0
		161	1	0	0	0	0	1	1	0	1	0	0	0
		163	1	1	0	0	0	1	1	0	1	0	0	0
		167	1	1	1	0	0	1	1	0	1	0	0	0
		144	0	0	1	0	0	0	1	0	1	0	0	0
		174	0	0	1	0	1	1	1	0	1	0	0	0
		167	1	1	1	0	0	1	1	0	1	0	0	0
		1A6	0	1	1	0	0	1	0	1	1	0	0	0

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MICROCHIP

27C256

15 bit Alamat

8 bit data

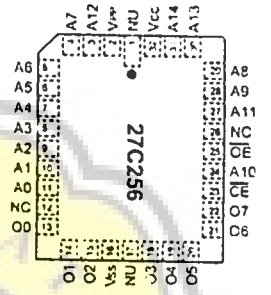
256K (32K x 8) CMOS EPROM

FEATURES

- High speed performance
  - 90 ns access time available
- CMOS Technology for low power consumption
  - 20 mA Active current
  - 100 µA Standby current
- Factory programming available
- Auto-Insertion-compatible plastic packages
- Auto ID aids automated programming
- Separate chip enable and output enable controls
- High speed "express" programming algorithm
- Organized 32K x 8: JEDEC standard pinouts
  - 28-pin Dual-in-line package
  - 32-pin PLCC Package
  - 28-pin SOIC package
  - Tape and reel
- Data Retention > 200 years
- Available for the following temperature ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C
  - Automotive: -40°C to +125°C

PACKAGE TYPES

PLCC



DIP/SOIC

DESCRIPTION

The Microchip Technology Inc. 27C256 is a CMOS 256 Kbit electrically Programmable Read Only Memory (EPROM). The device is organized as 32K words by 8 bits (32K bytes). Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 90 ns. This very high speed device allows the most sophisticated microprocessors to run at full speed without the need for WAIT states. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are requirements.

A complete family of packages is offered to provide the most flexibility in applications. For surface mount applications, PLCC, or SOIC packaging is available. Tape and reel packaging is also available for PLCC or SOIC packages.

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1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

Vcc and input voltages w.r.t. Vss ..... -0.6V to +7.25V

VPP voltage w.r.t. Vss during programming ..... -0.6V to +14.0V

Voltage on A9 w.r.t. Vss ..... -0.6V to +13.5V

Output voltage w.r.t. Vss ..... -0.6V to Vcc +1.0V

Storage temperature ..... -65°C to +150°C

Ambient temp. with power applied ..... -65°C to +125°C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0-A14	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
VPP	Programming Voltage
O0 - O7	Data Output
Vcc	+5V Power Supply
Vss	Ground
NC	No Connection; No Internal Connection
NU	Not Used; No External Connection Is Allowed

TABLE 1-2: READ OPERATION DC CHARACTERISTICS

Vcc = +5V (±10%)
Commercial: Tamb = 0°C to +70°C
Industrial: Tamb = -40°C to +85°C
Extended (Automotive): Tamb = -40°C to +125°C

Parameter	Part*	Status	Symbol	Min.	Max.	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.5	Vcc+1 0.8	V V	
Input Leakage	all	—	ILI	-10	10	µA	VIN = 0 to Vcc
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -400 µA IOL = 2.1 mA
Output Leakage	all	—	ILO	-10	10	µA	VOUT = 0V to Vcc
Input Capacitance	all	—	CIN	—	6	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz
Output Capacitance	all	—	COUT	—	12	pF	VOUT = 0V; Tamb = 25°C; f = 1 MHz
Power Supply Current, Active	C I,E	TTL input TTL input	ICC1 ICC2	— —	20 25	mA mA	Vcc = 5.5V; VPP = Vcc f = 1 MHz; $\overline{OE}$ = $\overline{CE}$ = VIL; IOUT = 0 mA; VIL = -0.1 to 0.8V; VIH = 2.0 to Vcc; Note 1
Power Supply Current, Standby	C I, E all	TTL input TTL input CMOS input	ICC(S)	—	2 3 100	mA mA µA	 $\overline{CE}$ = Vcc ± 0.2V
IPP Read Current	all	Read Mode	IPP		100	µA	VPP = 5.5V
VPP Read Voltage	all	Read Mode	VPP	Vcc-0.7	Vcc	V	

* Parts: C: Commercial Temperature Range; I, E=Industrial and Extended Temperature Ranges

Note 1: Typical active current increases .75 mA per MHz up to operating frequency for all temperature ranges.

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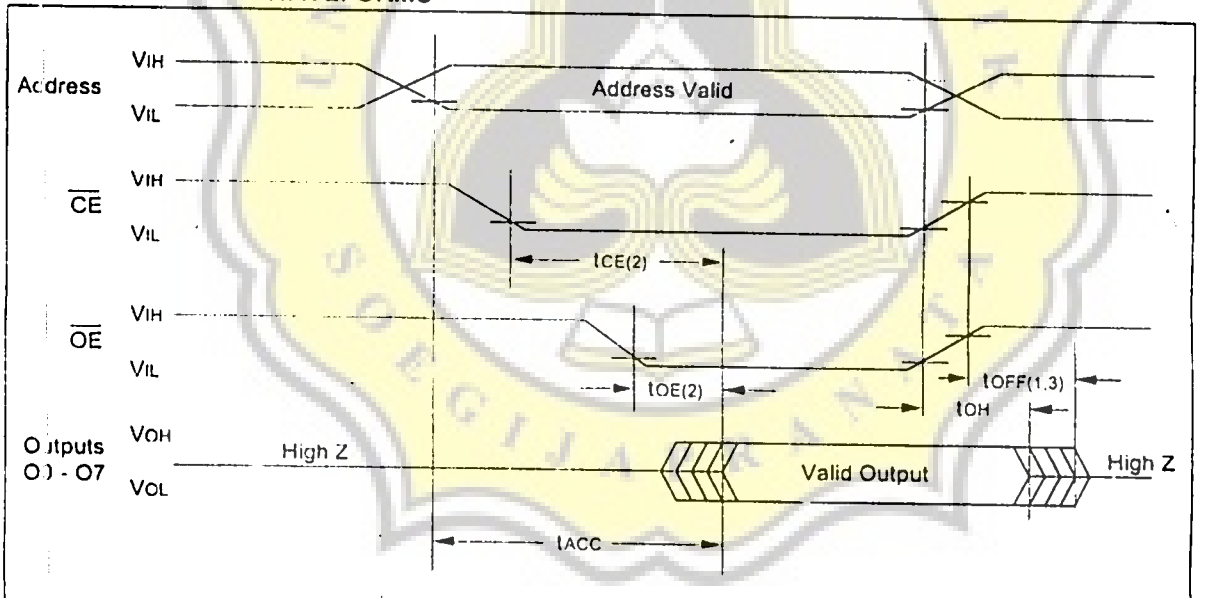
TABLE 1-3: READ OPERATION AC CHARACTERISTICS

AC Testing Waveform:	V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V V_{OL} = 0.8V	
Output Load:	1 TTL Load + 100 pF	
Input Rise and Fall Times:	10 ns	
Ambient Temperature:	Commercial:	Tamb = 0°C to +70°C
	Industrial:	Tamb = -40°C to +85°C
	Automotive:	Tamb = -40°C to +125°C

Parameter	Sym	27C256-90*		27C256-10*		27C256-12		27C256-15		27C256-20		Units	Conditions
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Address to Output Delay	tACC	—	90	—	100	—	120	—	150	—	200	ns	$\overline{CE}$=$\overline{OE}$ =V_{IL}
$\overline{CE}$ to Output Delay	tCE	—	90	—	100	—	120	—	150	—	200	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	tOE	—	40	—	45	—	55	—	65	—	75	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	tOFF	0	30	0	30	0	35	0	50	0	55	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever goes first	tOH	0	—	0	—	0	—	0	—	0	—	ns	

* -10, -90 AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = .45V; V_{OH} = 1.5V and V_{OL} = 1.5V
Output Load: 1 TTL Load + 30pF

FIGURE 1-1: READ WAVEFORMS

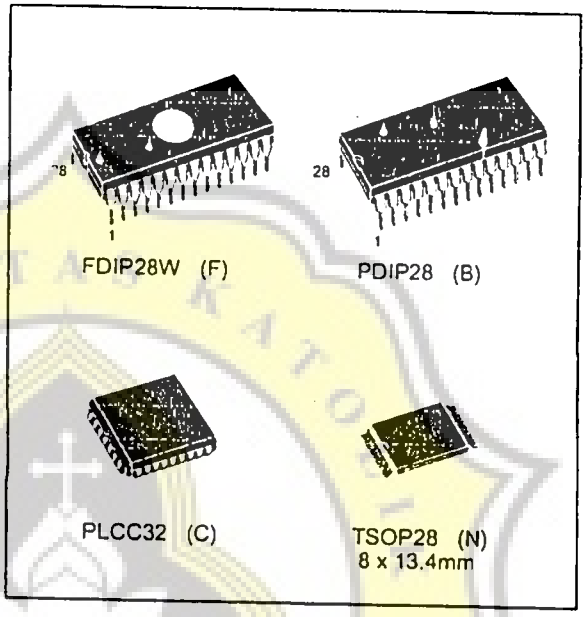


Notes: (1) tOFF is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to tCE - tOE after the falling edge of $\overline{CE}$ without impact on tCE
(3) This parameter is sampled and is not 100% tested.

M27C512

512 Kbit (64Kb x8) UV EPROM and OTP EPROM

- 5V ± 10% SUPPLY VOLTAGE in READ OPERATION
- FAST ACCESS TIME: 45ns
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 30mA
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.75V ± 0.25V
- PROGRAMMING TIMES of AROUND 6sec. (PRESTO IIB ALGORITHM)
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 20h
  - Device Code: 3Dh



DESCRIPTION

The M27C512 is a 512 Kbit EPROM offered in the two ranges UV (ultra violet erase) and OTP (one time programmable). It is ideally suited for applications where fast turn-around and pattern experimentation are important requirements and is organized as 65,536 by 8 bits.

The FDIP28W (window ceramic frit-seal package) has transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27C512 is offered in PDIP28, PLCC32 and TSOP28 (8 x 13.4 mm) packages.

Figure 1. Logic Diagram

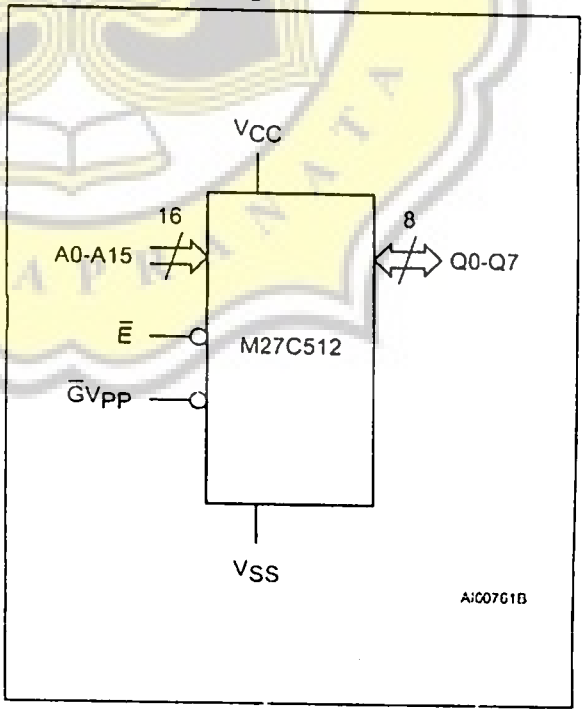


Table 1. Signal Names

A0-A15	Address Inputs
Q0-Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}V_{PP}$	Output Enable / Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

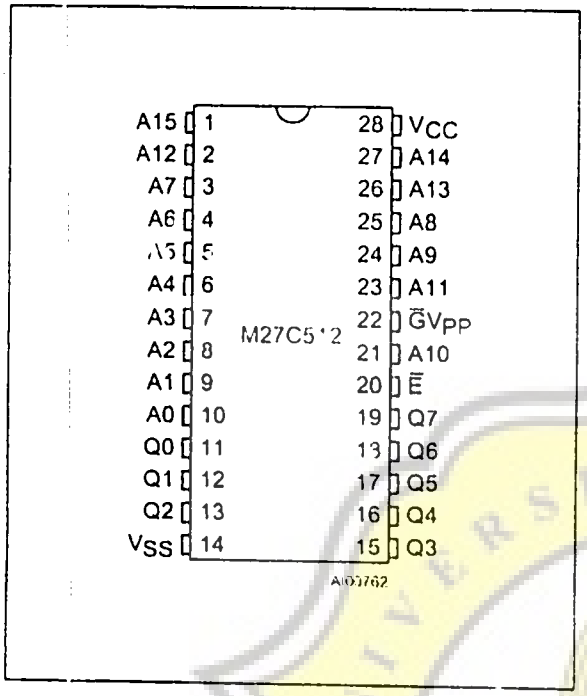
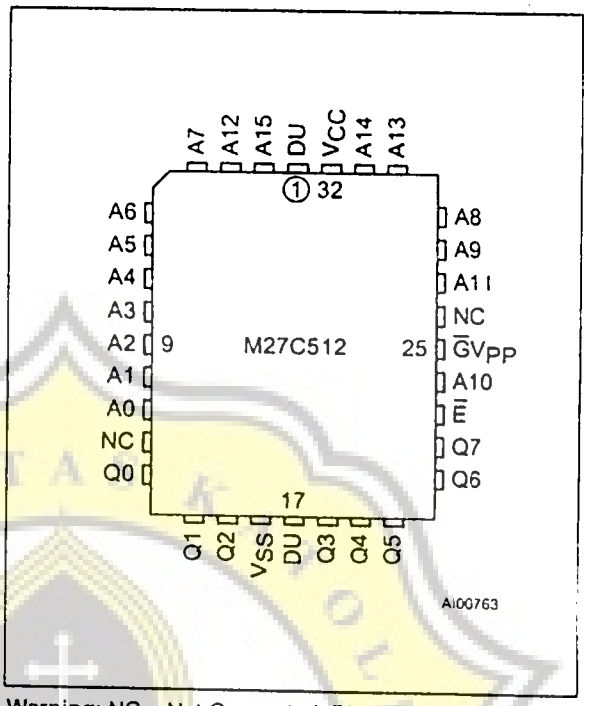
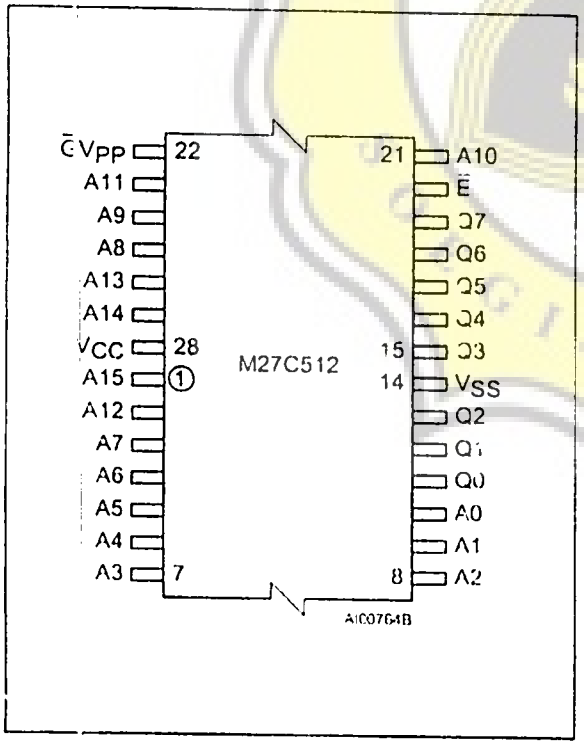


Figure 2B. LCC Pin Connections



Warning: NC = Not Connected, DU = Don't Use

Figure 2C. TSOP Pin Connections



DEVICE OPERATION

The modes of operations of the M27C512 are listed in the Operating Modes table. A single power supply is required in the read mode. All inputs are TTL levels except for $\overline{G}V_{PP}$ and 12V on A9 for Electronic Signature.

Read Mode

The M27C512 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27C512 has a standby mode which reduces the active current from 30mA to 100µA The M27C512 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}V_{PP}$ input.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature (3)	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.
3. Depends on range.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}V_{PP}$	A9	Q0 - Q7
Read	V_{IL}	V_{IL}	X	Data Out
Output Disable	V_{IL}	V_{IH}	X	Hi-Z
Program	V_{IL} Pulse	V_{PP}	X	Data In
Program Inhibit	V_{IH}	V_{PP}	X	Hi-Z
Standby	V_{IH}	X	X	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{ID}	Codes

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	0	1	1	1	1	0	1	3Dh

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

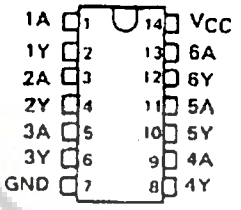
For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

SN5414, SN54LS14, SN7414, SN74LS14
HEX SCHMITT-TRIGGER INVERTERS

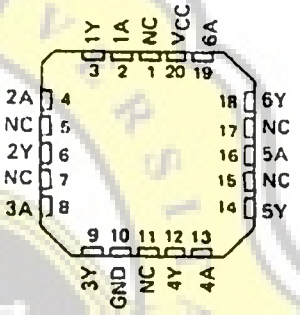
DECEMBER 1983 – REVISED MARCH 1988

- Operation from Very Slow Edges
- Improved Line-Receiving Characteristics
- High Noise Immunity

SN5414, SN54LS14 . . . J OR W PACKAGE
SN7414 . . . N PACKAGE
SN74LS14 . . . D OR N PACKAGE
(TOP VIEW)



SN54LS14 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

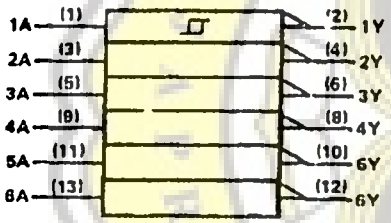
description

Each circuit functions as an inverter, but because of the Schmitt action, it has different input threshold levels for positive (V_{T+}) and for negative going (V_{T-}) signals.

These circuits are temperature-compensated and can be triggered from the slowest of input ramps and still give clean, jitter-free output signals.

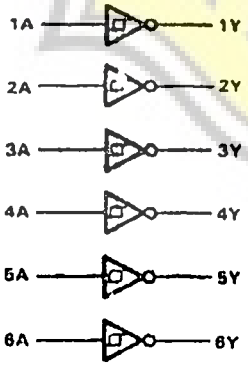
The SN5414 and SN54LS14 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7414 and the SN74LS14 are characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

logic diagram (positive logic)



$Y = \overline{A}$

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS INSTRUMENTS
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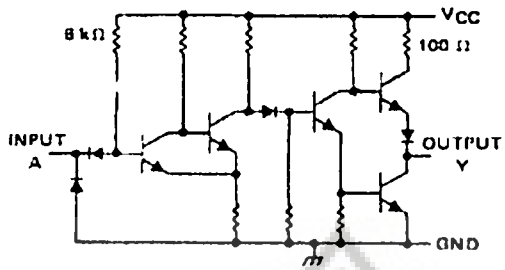
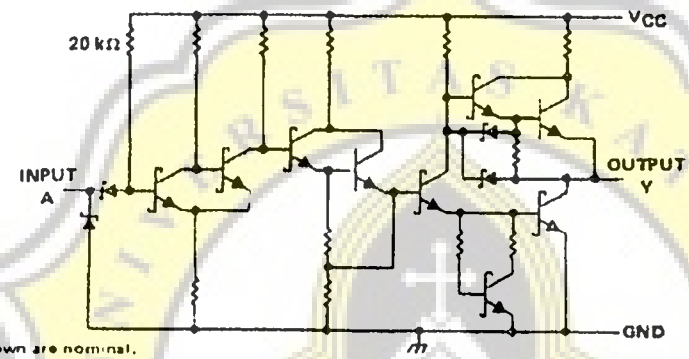
schematics

'14



'LS14



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)		7 V
Input voltage: '14		5.5 V
'LS14		7 V
Operating free-air temperature:	SN54'	−55°C to 125°C
	SN74'	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN5414			SN7414			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH} High-level output current			−0.8			−0.8	mA
I_{OL} Low-level output current			16			16	mA
T_A Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{T+}	V_{CC} = 5 V			1.5	1.7	2	V
V_{T-}	V_{CC} = 5 V			0.6	0.9	1.1	V
Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = 5 V			0.4	0.8		V
V_{IK}	V_{CC} = MIN,	I_I = −12 mA				−1.5	V
V_{OH}	V_{CC} = MIN,	V_I = 0.8 V,	I_{OH} = −0.8 mA	2.4	3.4		V
V_{OL}	V_{CC} = MIN,	V_I = 2 V,	I_{OL} = 16 mA		0.2	0.4	V
I_{T+}	V_{CC} = 5 V,	$V_I = V_{T+}$			−0.43		mA
I_{T-}	V_{CC} = 5 V,	$V_I = V_{T-}$			−0.56		mA
I_I	V_{CC} = MAX,	V_I = 5.5 V				1	mA
I_{IH}	V_{CC} = MAX,	V_{IH} = 2.4 V				40	μA
I_{IL}	V_{CC} = MAX,	V_{IL} = 0.4 V			−0.8	−1.2	mA
I_{OS}§	V_{CC} = MAX			−18		−55	mA
I_{CCH}	V_{CC} = MAX				22	38	mA
I_{CCL}	V_{CC} = MAX				39	60	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A	Y	R_L = 400 Ω,	C_L = 15 pF		15	22	ns
t_{PHL}						15	22	ns

recommended operating conditions

		SN54LS14			SN74LS14			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

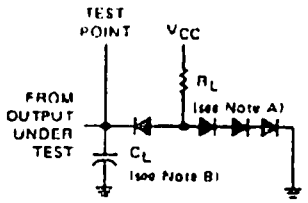
PARAMETER	TEST CONDITIONS†			SN54LS14			SN74LS14			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{T+}	V_{CC} = 5 V			1.4	1.6	1.9	1.4	1.6	1.9	V
V_{T-}	V_{CC} = 5 V			0.5	0.8	1	0.5	0.8	1	V
Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = 5 V			0.4	0.8		0.4	0.8		V
V_{IK}	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	V_{CC} = MIN,	V_I = 0.5 V,	I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN,	V_I = 1.9 V	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_{T+}	V_{CC} = 5 V,	$V_I = V_{T+}$			−0.14			−0.14		mA
I_{T-}	V_{CC} = 5 V,	$V_I = V_{T-}$			−0.18			−0.18		mA
I_I	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}	V_{CC} = MAX,	V_{IH} = 2.7 V				20			20	μA
I_{IL}	V_{CC} = MAX,	V_{IL} = 0.4 V				−0.4			−0.4	mA
I_{OS}§	V_{CC} = MAX			−20		−100	−20		−100	mA
I_{CCH}	V_{CC} = MAX				8.6	18		8.6	18	mA
I_{CCL}	V_{CC} = MAX				12	21		12	21	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ No more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

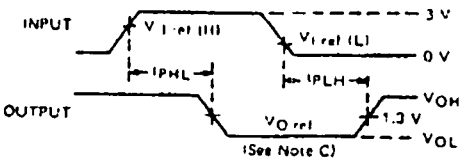
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A	Y	R_L = 2 kΩ,	C_L = 15 pF		15	22	ns
t_{PHL}						18	22	ns

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

NOTES. A. All diodes are 1N3064 or equivalent.
B. C_L includes probe and jig capacitance.
C. Generator characteristics and reference voltage are:

	Generator Characteristics				Reference Voltages		
	Z_{out}	PRR	t_r	t_f	$V_{I\,ref(H)}$	$V_{I\,ref(L)}$	$V_{O\,ref}$
SN54'/SN74'	50 Ω	1 MHz	10 ns	10 ns	1.7 V	0.9 V	1.5 V
SN54LS'/SN74LS'	50 Ω	1 MHz	15 ns	6 ns	1.6 V	0.8 V	1.3 V

TYPICAL CHARACTERISTICS OF '14 CIRCUITS

POSITIVE-GOING THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

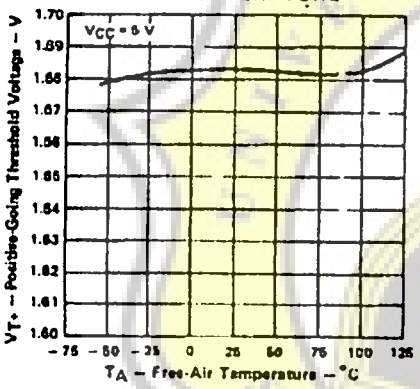


FIGURE 1

NEGATIVE-GOING THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

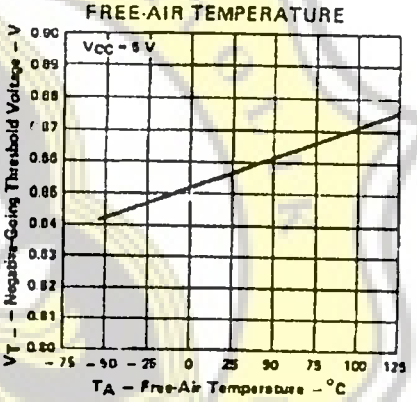


FIGURE 2

HYSTERESIS
vs
FREE-AIR TEMPERATURE

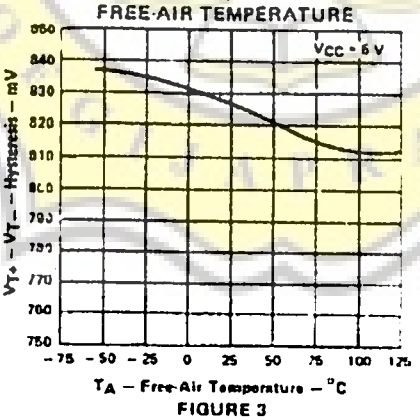


FIGURE 3

Data for temperatures below 0°C and 70°C and supply voltages below 4.75V and above 5.25 V are applicable for SN5414 only.

TYPICAL CHARACTERISTICS OF '14 CIRCUITS

DISTRIBUTION OF UNITS FOR HYSTERESIS

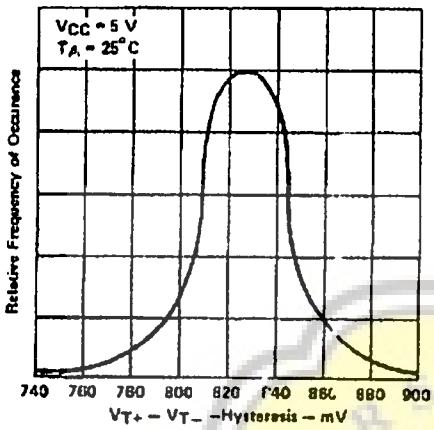


FIGURE 4

THRESHOLD VOLTAGES vs SUPPLY VOLTAGE

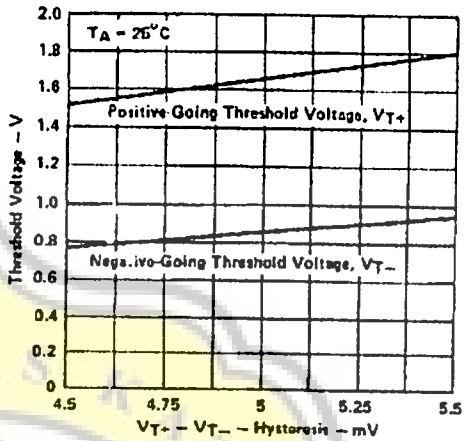


FIGURE 5

HYSTERESIS vs SUPPLY VOLTAGE

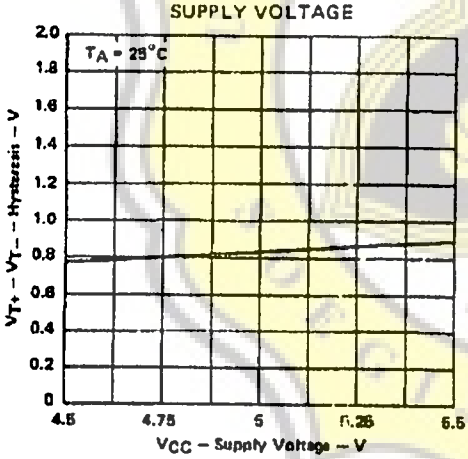


FIGURE 6

OUTPUT VOLTAGE vs INPUT VOLTAGE

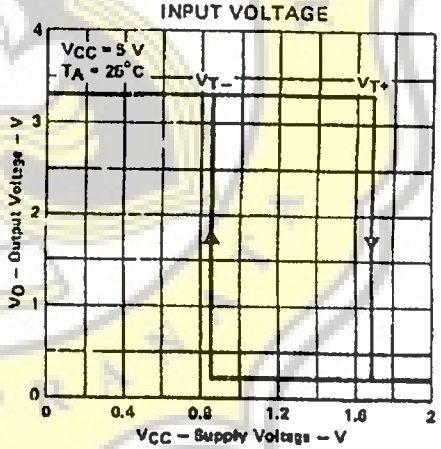


FIGURE 7

Data for temperatures below 0°C and 70°C and supply voltages below 4.75 V and above 5.25 V are applicable for SN5414 only.

TYPICAL CHARACTERISTICS OF 'LS14 CIRCUITS

POSITIVE-GOING THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

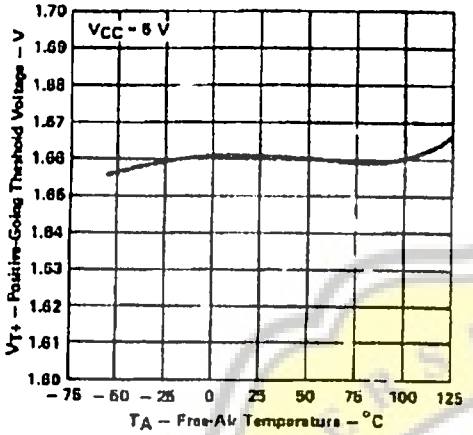


FIGURE 8

NEGATIVE-GOING THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

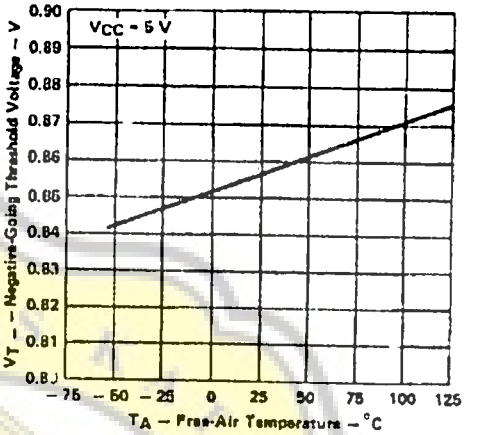


FIGURE 9

HYSTERESIS
vs
FREE-AIR TEMPERATURE

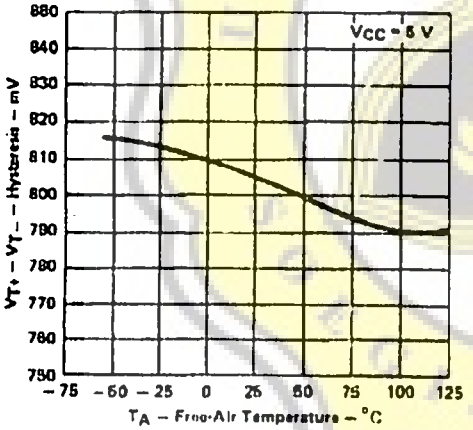


FIGURE 10

DISTRIBUTION OF UNITS
FOR HYSTERESIS

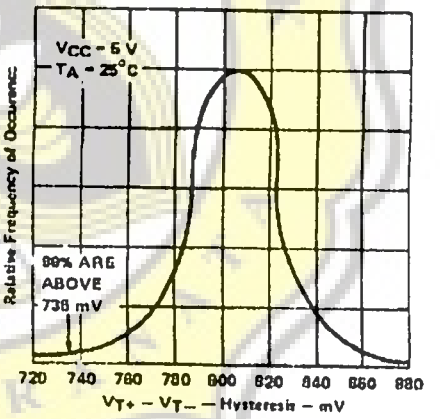


FIGURE 11

Data for temperatures below 0°C and above 70°C and supply voltages below 4.75 V and above 5.25 V are applicable for SN54LS14 only.

TYPICAL CHARACTERISTICS OF 'LS14 CIRCUITS

THRESHOLD VOLTAGES AND HYSTERESIS
vs
SUPPLY VOLTAGE

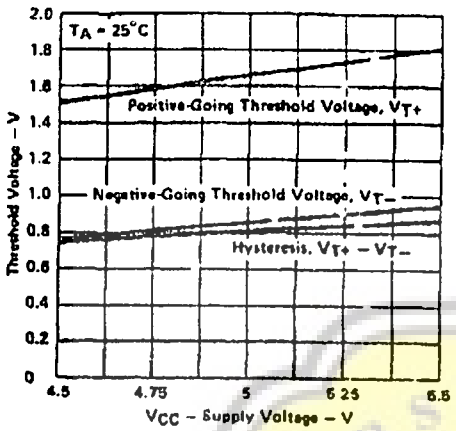


FIGURE 12

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

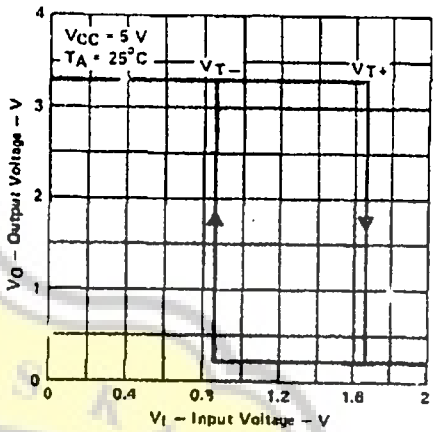
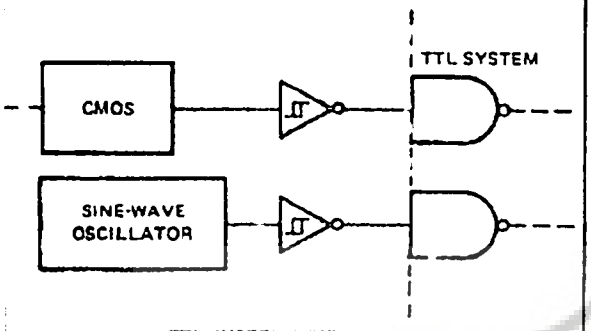


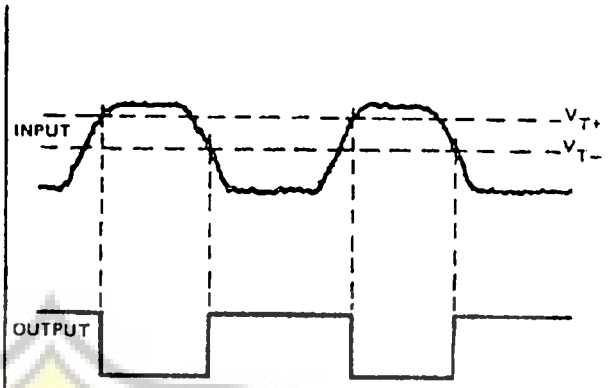
FIGURE 13

Data for temperatures below 0°C and above 70°C and supply voltages below 4.75 V and above 5.25 V are applicable for SN54LS14 only.

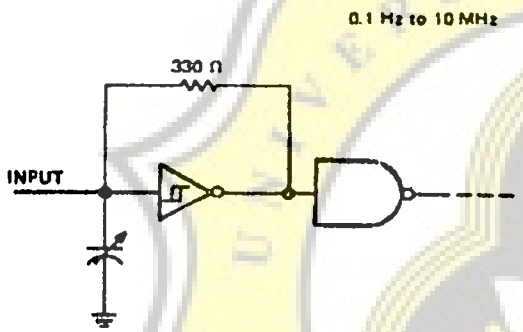
TYPICAL APPLICATION DATA



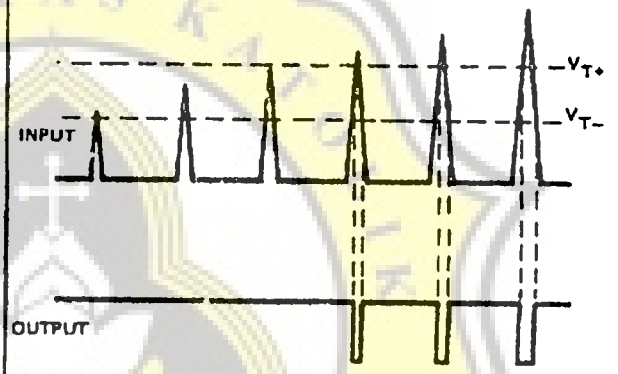
TTL SYSTEM INTERFACE FOR SLOW INPUT WAVEFORMS



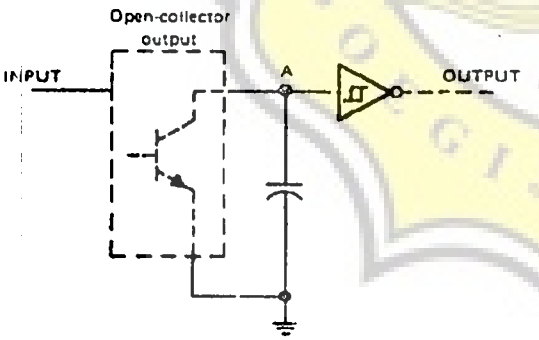
PULSE SHAPER

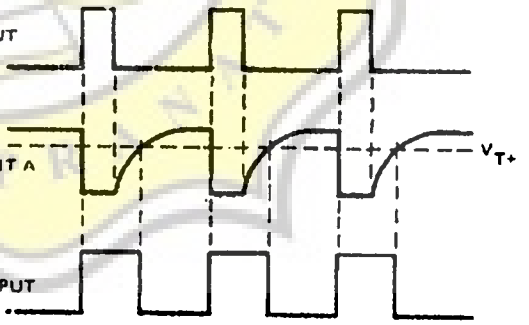


MULTIVIBRATOR



THRESHOLD DETECTOR





PULSE STRETCHER

eneral purpose CMOS timer ICM7555

CRIPTION

M7555 is a CMOS timer providing significantly improved mance over the standard NE/SE555 timer, while at the same eing a direct replacement for those devices in most ations. Improved parameters include low supply current, wide ing supply voltage range, low THRESHOLD, TRIGGER, and T currents, no crowbarring of the supply current during output ions, higher frequency performance and no requirement to ple CONTROL VOLTAGE for stable operation.

M7555 is a stable controller capable of producing accurate elays or frequencies.

one-shot mode, the pulse width of each circuit is precisely lled by one external resistor and capacitor. For astable ion as an oscillator, the free-running frequency and the duty are both accurately controlled by two external resistors and apacitor. Unlike the bipolar 555 device, the CONTROL AGE terminal need not be decoupled with a capacitor. The GER and RESET inputs are active low. The output inverter can or sink currents large enough to drive TTL loads or provide at offsets to drive CMOS loads.

TURES

ct equivalent in most applications for NE/SE555

supply current: 80µA (typ)

emely low trigger, threshold, and reset currents: 20pA (typ)

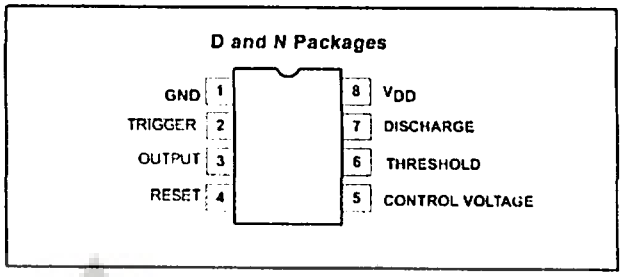
-speed operation: 500kHz guaranteed

e operating supply voltage range guaranteed 3 to 16V over full motive temperatures

mal reset function; no crowbarring of supply during output sition

be used with higher-impedance timing elements than the lar 555 for longer time constants

PIN CONFIGURATION



- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- High output source/sink driver can drive TTL/CMOS
- Typical temperature stability of 0.005%/°C at 25°C
- Rail-to-rail outputs

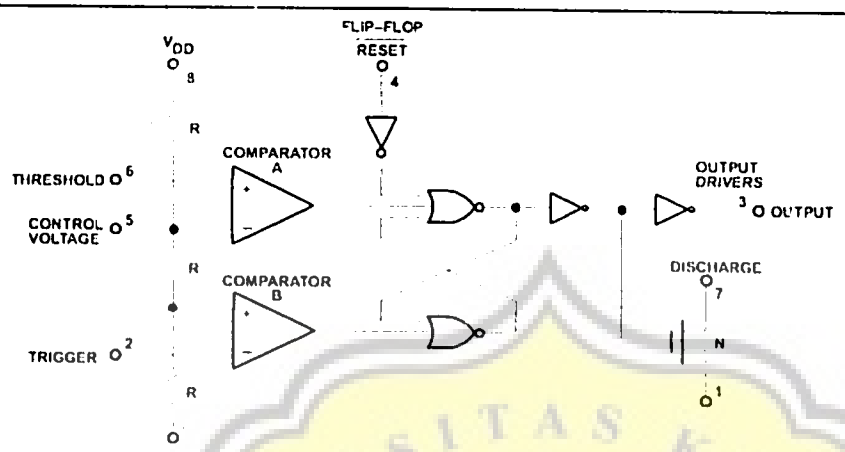
APPLICATIONS

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Missing pulse detector

ERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
Plastic Dual In-Line Package (DIP)	0 to +70°C	ICM7555CN	0404B
Plastic Small Outline (SO) Package	0 to +70°C	ICM7555CD	0174C
Plastic Dual In-Line Package (DIP)	-40 to +85°C	ICM7555IN	0404B
Plastic Small Outline (SO) Package	-40 to +85°C	ICM7555ID	0174C

JIVALENT BLOCK DIAGRAM



OTE
NUSED INPUTS SHOULD BE CONNECTED TO APPROPRIATE VOLTAGE FROM TRUTH TABLE.

ITH TABLE

RESHOLD VOLTAGE	TRIGGER VOLTAGE	RESET[1]	OUTPUT	DISCHARGE SWITCH
DON'T CARE	DON'T CARE	LOW	LOW	ON
>2/3(V+)	> 1/3(V+)	HIGH	LOW	ON
V_{TH} < 2/3	V_{TR} > 1/3	HIGH	STABLE	STABLE
DON'T CARE	<1/3(V+)	HIGH	HIGH	OFF

ES:
ESET will dominate all other inputs. TRIGGER will dominate over THRESHOLD.

SOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNITS
V_{DD}	Supply voltage	+18	V
V_{TRIG}[1]	Trigger input voltage		
V_{CV}	Control voltage	> -0.3 to	
V_{TH}	Threshold input voltage	<V_{DD} + 0.3	V
V_{RST}	RESET input voltage		
I_{OUT}	Output current	100	mA
P_{DMAX}	Maximum power dissipation, T_A = 25°C (still air)[2]		
	N package	1160	mW
	D package	780	mW
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead temperature (Soldering 60s)	300	°C

ES:
ue to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than
DD + 0.3V or less than GND -0.3V may cause destructive latch-up. For this reason it is recommended that no inputs from external sources
t operating from the same power supply be applied to the device before its power supply is established. In multiple systems, the supply of
e ICM7555 must be turned on first.
erate above 25°C, at the following rates:
N package at 9.3mW/°C
D package at 6.2mW/°C
ee "Power Dissipation Considerations" section.

DC AND AC ELECTRICAL CHARACTERISTICS

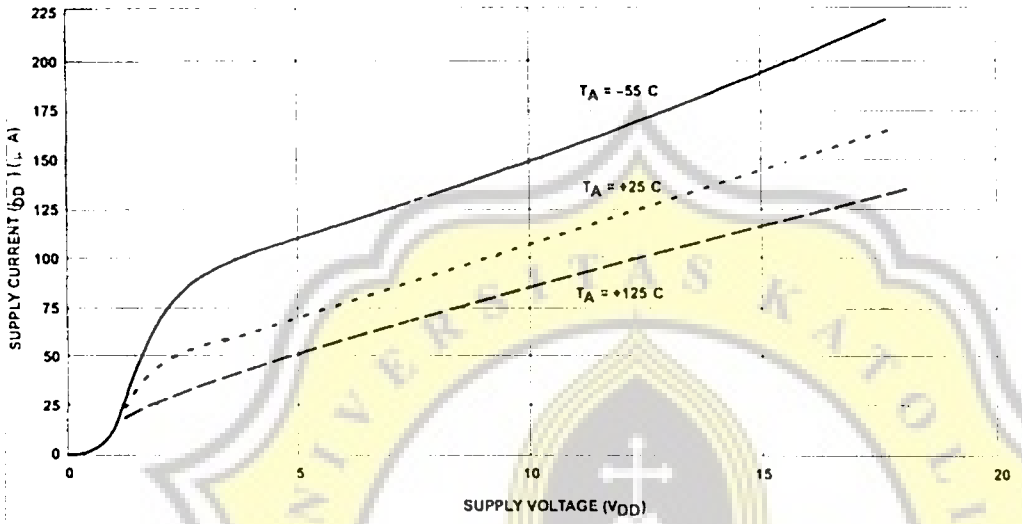
T_A = 25°C unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS ICM7555 MIN	TYP	MAX	UNITS
V_{DD}	Supply voltage	$T_{MIN} \le T_A \le T_{MAX}$	3		16	V
I_{DD}	Supply current[1]	$V_{DD} = V_{MIN}$ $V_{DD} = V_{MAX}$		50 180	200 300	µA µA
	Astable mode timing[2] Initial accuracy Drift with supply voltage Drift with temperature[3]	R_A, R_B = 1k to 100k, C = 0.1µF 5V < V_{DD} < 15V V_{DD} = 5V V_{DD} = 10V V_{DD} = 15V		 1.0 0.1 50 75 100	 5.0 3.0	 % %/V ppm/°C ppm/°C ppm/°C
V_{TH}	Threshold voltage	V_{DD} = 5V	0.63	0.65	0.67	xV_{DD}
V_{TRIG}	Trigger voltage	V_{DD} = 5V	0.29	0.31	0.34	xV_{DD}
I_{TRIG}	Trigger current	$V_{DD} = V_{TRIG} = V_{MAX}$ $V_{DD} = V_{TRIG}$ = 5V $V_{DD} = V_{TRIG} = V_{MIN}$		50 10 1		pA pA pA
I_{TH}	Threshold current	$V_{DD} = V_{TH} = V_{MAX}$ $V_{DD} = V_{TH}$ = 5V $V_{DD} = V_{TH} = V_{MIN}$		50 10 1		pA pA pA
I_{RST}	Reset current	$V_{DD} = V_{RST} = V_{MAX}$ $V_{DD} = V_{RST}$ = 5V $V_{DD} = V_{RST} = V_{MIN}$		100 20 2		pA pA pA
V_{RST}	Reset voltage	$V_{DD} = V_{MIN}$ and V_{MAX}	0.4	0.7	1.0	V
V_{CL}	Control voltage	V_{DD} = 5V	0.62	0.65	0.67	xV_{DD}
V_{OL}	Output voltage (low)	$V_{DD} = V_{MAX}$, I_{SINK} = 3.2mA V_{DD} = 5V, I_{SINK} = 3.2mA		0.1 0.2	0.4 0.4	V V
V_{OH}	Output voltage (high)	$V_{DD} = V_{MAX}$, I_{SOURCE} = -1.0mA V_{DD} = 5V, I_{SOURCE} = -1.0mA	15.25 4.0	15.7 4.5		V_{DD} V_{DD}
V_{DIS}	Discharge output voltage	V_{DD} = 5V, I_{DIS} = 10.0mA		0.2	0.4	V
t_R	Rise time of output[3]	R_L = 10MΩ, C_L = 10pF, V_{DD} = 5V		45	75	ns
t_F	Fall time of output[3]	R_L = 10MΩ, C_L = 10pF, V_{DD} = 5V		20	75	ns
F_{MAX}	Maximum oscillator frequency (astable mode)		500			kHz

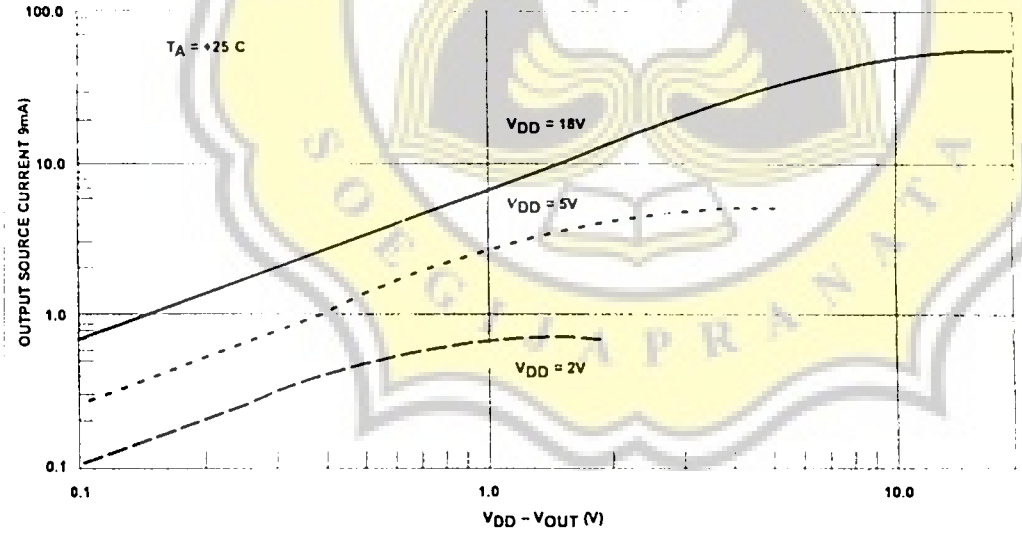
NOTES:

1. The supply current value is essentially independent of the TRIGGER, THRESHOLD, and RESET voltages.
2. Astable timing is calculated using the following equation: $f = \frac{1.38}{(R_A + 2R_B)C}$. The components are defined in Figure 2.
3. Parameter is not 100% tested.

CAL PERFORMANCE CHARACTERISTICS



Supply Current vs Supply Voltage



High Output Voltage Drop vs Output Source Current

FAIRCHILD SEMICONDUCTOR™

August 1986
Revised July 2001

DM7408
Quad 2-Input AND Gates

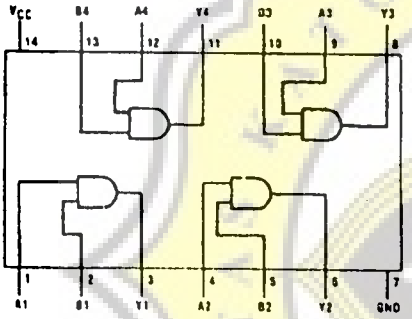
General Description

This device contains four independent gates each of which performs the logic AND function.

Ordering Code:

Order Number	Package Number	Package Description
DM7408N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Connection Diagram



Function Table

$Y = AB$

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = HIGH Logic Level
L = LOW Logic Level

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Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parameter values defined in the "Electrical Characteristics" tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.8	mA
I_{OL}	LOW Level Output Current			16	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.4	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min		0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	18		−55	mA
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max		11	21	mA
I_{CCL}	Supply Current with Outputs LOW	V_{CC} = Max		20	33	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	C_L = 15 pF, R_L = 400Ω		27	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output			19	ns

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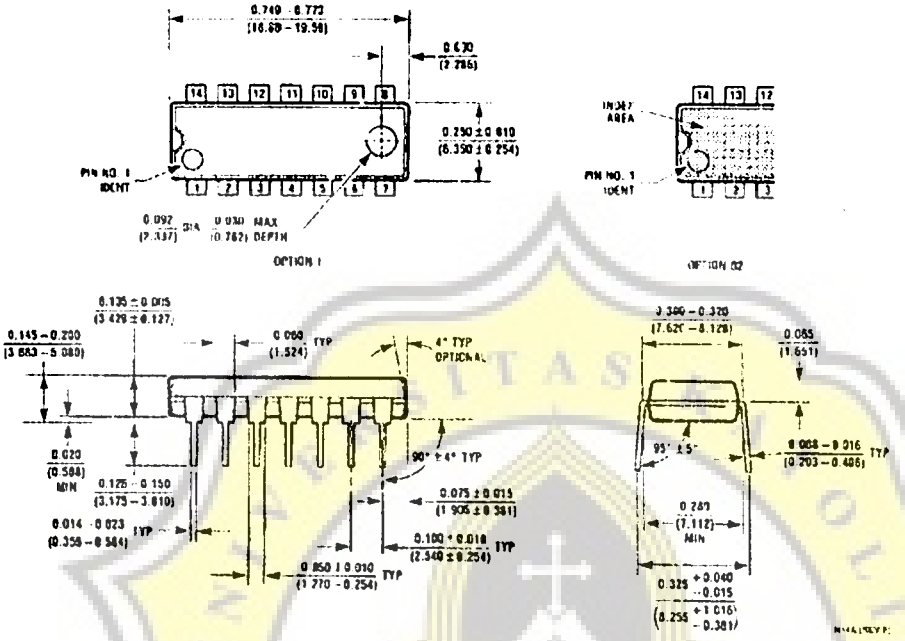
Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

SDLS119 – DECEMBER 1983 – REVISED MARCH 1988

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

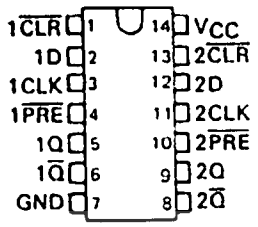
The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

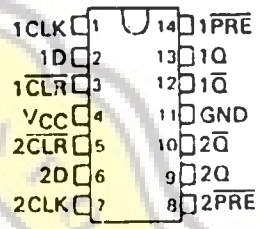
INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

† The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at preset and clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

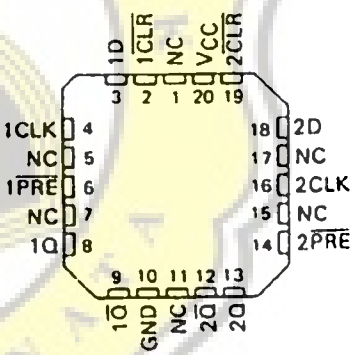
SN5474 . . . J PACKAGE
SN54LS74A, SN54S74 . . . J OR W PACKAGE
SN7474 . . . N PACKAGE
SN74LS74A, SN74S74 . . . D OR N PACKAGE
(TOP VIEW)



SN5474 . . . W PACKAGE
(TOP VIEW)

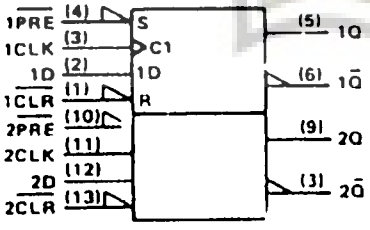


SN54LS74A, SN54S74 . . . FK PACKAGE
(TOP VIEW)



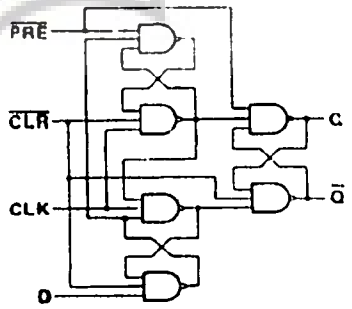
NC - No internal connection

logic symbol‡



‡This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

logic diagram (positive logic)



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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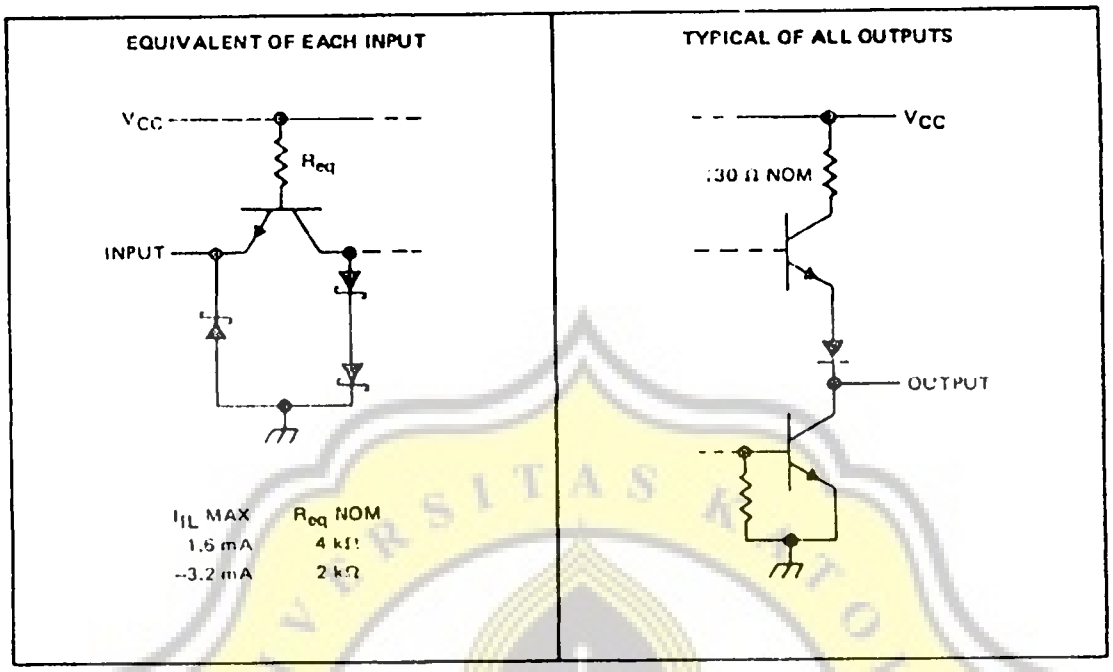
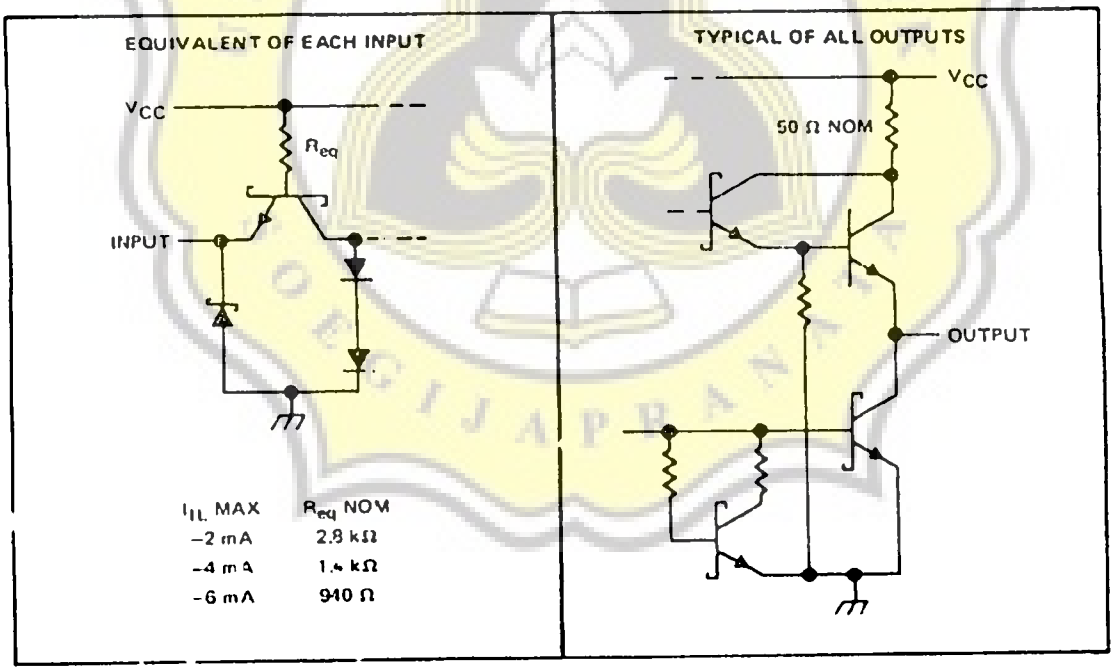
schematics of inputs and outputs

'74

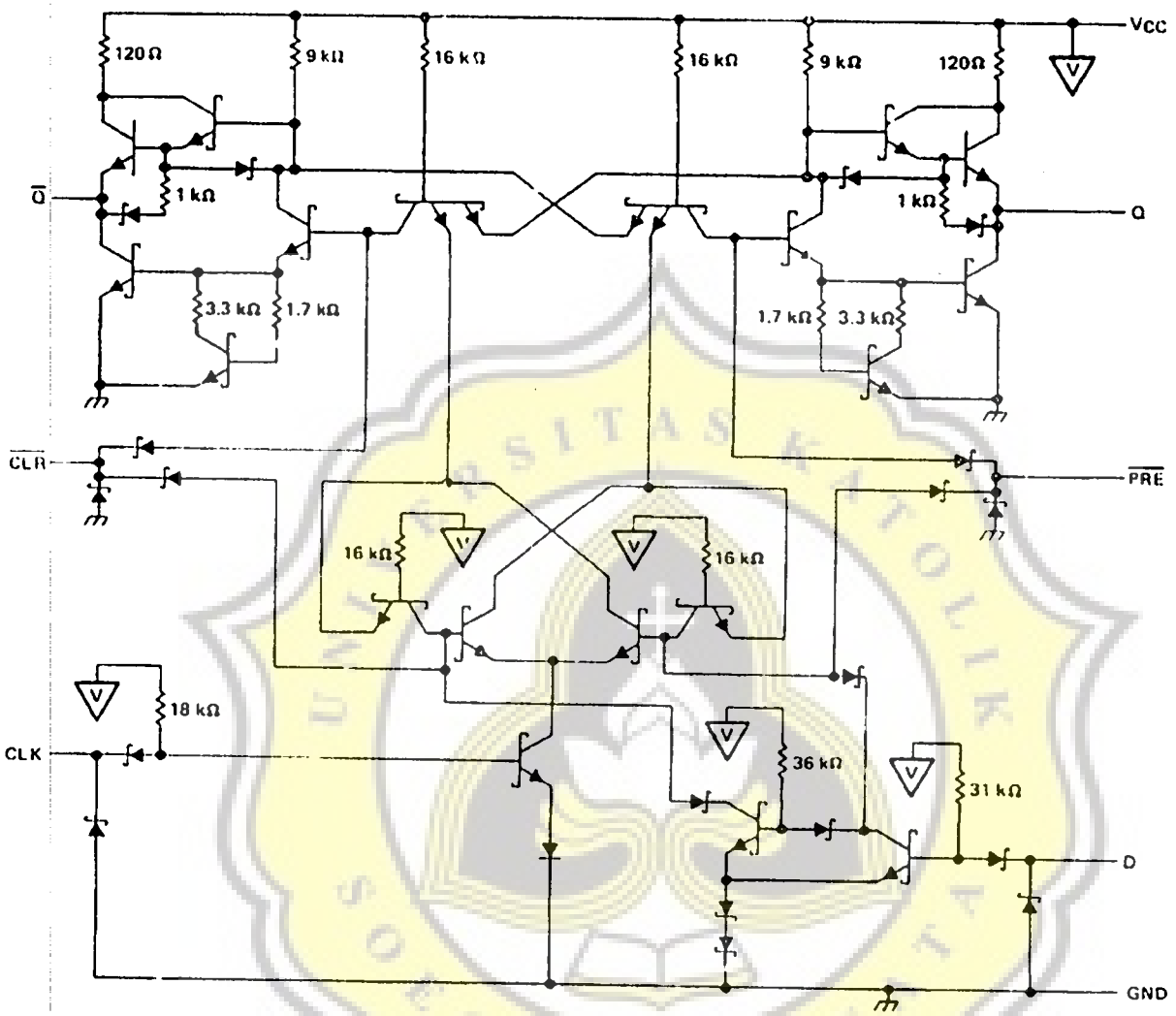


'S74



schematic

'LS74A



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '74, 'S74	5.5 V
'LS74A	7 V
Operating free-air temperature range: SN54'	−55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN5474 MIN	SN5474 NOM	SN5474 MAX	SN7474 MIN	SN7474 NOM	SN7474 MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				16			16	mA
t_w	Pulse duration	CLK high	30			30			ns
		CLK low	37			37			
		$\overline{PRE}$ or $\overline{CLR}$ low	30			30			
t_{su}	Input setup time before CLK↑		20			20			ns
t_h	Input hold time-data after CLK↑		5			5			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN5474 MIN	SN5474 TYP‡	SN5474 MAX	SN7474 MIN	SN7474 TYP‡	SN7474 MAX	UNIT
V_{IK}		V_{CC} = MIN,	I_I = −12 mA				−1.5			−1.5	V
V_{OH}		V_{CC} = MIN, I_{OH} = −0.4 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V,	2.4	3.4		2.4	3.4		V
V_{OL}		V_{CC} = MIN, I_{OL} = 16 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V,		0.2	0.4		0.2	0.4	V
I_I		V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	D	V_{CC} = MAX,	V_I = 2.4 V				40			40	μA
	$\overline{CLR}$						120			120	
	All Other						80			80	
I_{IL}	D	V_{CC} = MAX,	V_I = 0.4 V				−1.6			−1.6	mA
	$\overline{PRE}$§						−1.6			−1.6	
	$\overline{CLR}$§						−3.2			−3.2	
	CLK						−3.2			−3.2	
I_{OS}¶		V_{CC} = MAX			−20		−57	−18		−57	mA
I_{CC}#		V_{CC} = MAX,	See Note 2			8.5	15		8.5	15	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Clear is tested with preset high and preset is tested with clear high.
¶Not more than one output should be shorted at a time.
#Average per flip-flop.
NOTE 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

switching charateristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			R_L = 400 Ω, C_L = 15 pF	15	25		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$				25	ns
t_{PHL}						40	ns
t_{PLH}	CLK	Q or $\overline{Q}$			14	25	ns
t_{PHL}					20	40	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

recommended operating conditions

			SN54LS74A			SN74LS74A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		25	0		25	MHz
t_w	Pulse duration	CLK high	25			25			ns
		$\overline{PRE}$ or $\overline{CLR}$ low	25			25			
t_{su}	Setup time-before CLK↑	High-level data	20			20			ns
		Low-level data	20			20			
t_h	Hold time-data after CLK↑		5			5			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54LS74A			SN74LS74A			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}		V_{CC} = MIN, I_{OH} = −0.4 mA	V_{IH} = 2 V,	V_{IL} = MAX,	2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC} = MIN, I_{OL} = 4 mA	V_{IL} = MAX,	V_{IH} = 2 V,		0.25	0.4		0.25	0.4	V
		V_{CC} = MIN, I_{OL} = 8 mA	V_{IL} = MAX,	V_{IH} = 2 V,					0.35	0.5	
I_I	D or CLK	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
	$\overline{CLR}$ or $\overline{PRE}$						0.2			0.2	
I_{IH}	D or CLK	V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
	$\overline{CLR}$ or $\overline{PRE}$						40			40	
I_{IL}	D or CLK	V_{CC} = MAX,	V_I = 0.4 V				−0.4			−0.4	mA
	$\overline{CLR}$ or $\overline{PRE}$						−0.8			−0.8	
I_{OS}§		V_{CC} = MAX,	See Note 4		−20		−100	−20		−100	mA
I_{CC} (Total)		V_{CC} = MAX,	See Note 2			4	8		4	8	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.
NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V_O = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			R_L = 2 kΩ, C_L = 15 pF	25	33		MHz
t_{PLH}	$\overline{CLR}$, $\overline{PRE}$ or CLK	Q or $\overline{Q}$			13	25	ns
t_{PHL}					25	40	ns

Note 3: Load circuits and voltage waveforms are shown in Section 1.

mmended operating conditions

		SN54S74			SN74S74			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage		4.5	5	5.5	4.75	5	5.25	V
High-level input voltage		2			2			V
Low-level input voltage				0.8			0.8	V
High-level output current				– 1			– 1	mA
Low-level output current				20			20	mA
Pulse duration	CLK high	6			6			ns
	CLK low	7.3			7.3			
	$\overline{CLR}$ or $\overline{PRE}$ low	7			7			
Setup time, before CLK ↑	High-level data	3			3			ns
	Low-level data	3			3			
Input hold time - data after CLK ↑		2			2			ns
Operating free-air temperature		– 55		125	0		70	°C

trical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54S74			SN74S74			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
K		V_{CC} = MIN,	I_I = – 18 mA,				– 1.2			– 1.2	V
OH		V_{CC} = MIN, I_{OH} = – 1 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V,	2.5	3.4		2.7	3.4		V
OL		V_{CC} = MIN, I_{OL} = 20 mA	V_{IH} = 2 V	V_{IL} = 0.8 V,			0.5			0.5	V
		V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
H	D	V_{CC} = MAX,	V_I = 2.7 V				50			50	μA
	$\overline{CLR}$						150			150	
	$\overline{PRE}$ or CLK						100			100	
L	D	V_{CC} = MAX,	V_I = 0.5 V				– 2			– 2	mA
	$\overline{CLR}$¶						– 6			– 6	
	$\overline{PRE}$¶						– 4			– 4	
	CLK						– 4			– 4	
OS§		V_{CC} = MAX			– 40		– 100	– 40		– 100	mA
CC#		V_{CC} = MAX,	See Note 2			15	25		15	25	mA

r conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
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TE 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

itching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

ARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			R_L = 280 Ω, C_L = 15 pF	75	110		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$			4	6	ns
t_{PHL}	$\overline{PRE}$ or $\overline{CLR}$ (CLK high)	$\overline{Q}$ or Q			9	13.5	ns
	$\overline{PRE}$ or $\overline{CLR}$ (CLK low)				5	8	
t_{PLH}	CLK	Q or $\overline{Q}$			6	9	ns
t_{PHL}					6	9	ns

TE 3: Load circuits and voltage waveforms are shown in Section 1.

FAIRCHILD SEMICONDUCTOR™

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DM74123
Dual Retriggerable One-Shot with Clear and Complementary Outputs

General Description

The DM74123 is a dual retriggerable monostable multivibrator capable of generating output pulses from a few nano-seconds to extremely long duration up to 100% duty cycle. Each device has three inputs permitting the choice of either leading-edge or trailing edge triggering. Pin (A) is an active-LOW transition trigger input and pin (B) is an active-HIGH transition trigger input. A LOW at the clear (CLR) input terminates the output pulse: which also inhibits triggering. An internal connection from CLR to the input gate makes it possible to trigger the circuit by a positive-going signal on CLR as shown in the Truth Table.

To obtain the best and trouble free operation from this device please read the Operating Rules as well as the One–Shot Application Notes carefully and observe recommendations.

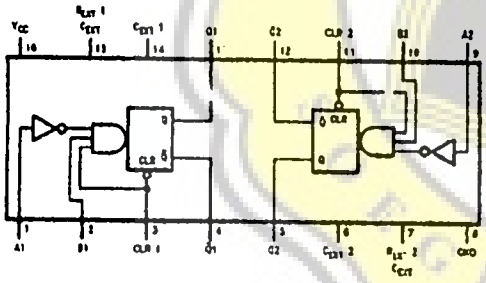
Features

- DC triggered from active-HIGH transition or active-LOW transition inputs
- Retriggerable to 100% duty cycle
- Direct reset terminates output pulse
- Compensated for V_{CC} and temperature variations
- DTL, TTL compatible
- Input clamp diodes

Ordering Code:

Order Number	Package Number	Package Description
DM74123N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Connection Diagram



Triggering Truth Table

Inputs			Response
A	B	CLR	
X	X	L	No Trigger
↘	L	X	No Trigger
↘	H	H	Trigger
H	↗	X	No Trigger
L	↗	H	Trigger
L	H	↗	Trigger

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Functional Description

The basic output pulse width is determined by selection of an external resistor (R_X) and capacitor (C_X). Once triggered, the basic pulse width may be extended by retriggering the gated active-LOW transition or active-HIGH transition inputs or be reduced by use of the active-LOW transition clear input. Retriggering to 100% duty cycle is possible by application of an input pulse train whose cycle time is shorter than the output cycle time such that a continuous "HIGH" logic state is maintained at the "Q" output.

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Operating Rules

1. An external resistor (R_X) and external capacitor (C_X) are required for proper operation. The value of C_X may vary from 0 to any necessary value. For small time constants high-grade mica, glass, polypropylene, polycarbonate, or polystyrene material capacitors may be used. For large time constants use tantalum or special aluminum capacitors. If the timing capacitors have leakages approaching 100 nA or if stray capacitance from either terminal to ground is greater than 50 pF the timing equations may not represent the pulse width the device generates.
2. When an electrolytic capacitor is used for C_X a switching diode is often required for standard TTL or e-shots to prevent high inverse leakage current (Figure 1). However, its use in general is not recommended with retriggerable operation.
3. The output pulse width (T_W) for C_X > 1000 pF is defined as follows:

   $t_W = K R_X C_X(1 + 0.7/R_X)$

   1. where: [R_X is in Kilo-ohm]

      [C_X is in pico Farad]

      [T_W is in nano second]

      [K ≈ 0.28]

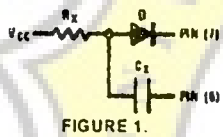


FIGURE 1.

4. For C_X < 1000 pF see Figure 2 for T_W vs. C_X family curves with R_X as a parameter:

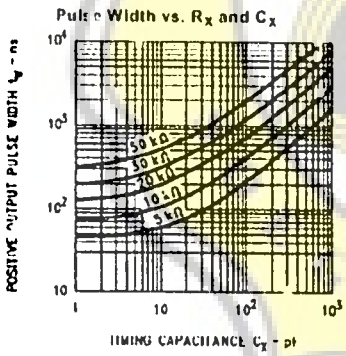
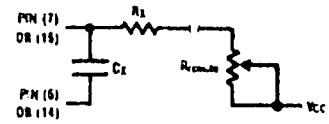


FIGURE 2.

5. To obtain variable pulse width by remote trimming, the following circuit is recommended:



Note: "R_{remote}" should be as close to the one-shot as possible

FIGURE 3.

6. The retriggerable pulse width is calculated as shown below:

   $T = T_W + t_{PLH} = K \times R_X \times C_X + t_{PLH}$

   The retriggered pulse width is equal to the pulse width plus a delay time period (Figure 4).

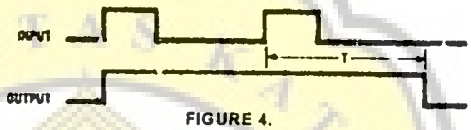


FIGURE 4.

7. Under any operating condition C_X and R_X must be kept as close to the one-shot device pins as possible to minimize stray capacitance, to reduce noise pick-up, and to reduce I × R and Ldi/dt voltage developed along their connecting paths. If the lead length from C_X to pins (6) and (7) or pins (14) and (15) is greater than 3 cm, for example, the output pulse width might be quite different from values predicted from the appropriate equations. A non-inductive and low capacitive path is necessary to ensure complete discharge of C_X in each cycle of its operation so that the output pulse width will be accurate.
8. V_{CC} and ground wiring should conform to good high-frequency standards and practices so that switching transients on the V_{CC} and ground return leads do not cause interaction between one-shots. A 0.01 µF to 0.10 µF bypass capacitor (disk ceramic or monolithic type) from V_{CC} to ground is necessary on each device. Furthermore, the bypass capacitor should be located as close to the V_{CC} pin as space permits.

Note: For further detailed device characteristics and output performance please refer to the One-Shot Application Note, AN-366.

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage		2			V
V_{IL}	LOW Level Input Voltage				0.8	V
I_{OH}	HIGH Level Output Current				−0.8	mA
I_{OL}	LOW Level Output Current				16	mA
t_W	Pulse Width (Note 2)	A or B HIGH	40			ns
		A or B LOW	40			
		Clear LOW	40			
T_{WQ} (Min)	Minimum Width of Pulse at Q (Note 2)	A or B			65	ns
R_{EXT}	External Timing Resistor		5		50	kΩ
C_{EXT}	External Timing Capacitance			No Restriction		μF
C_{WIRE}	Wiring Capacitance at R_{EXT}/C_{EXT} Terminal (Note 2)				50	pF
T_A	Free Air Operating Temperature		0		70	°C

Note 2: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.5	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.4V	Data			40	μA
			Clear			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Clear			−3.2	mA
			Data			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 4)		−10		−40	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 5)(Note 6)			38	66	mA

Note 3: All typicals are at V_{CC} = 5V, T_A = 25°C

Note 4: Not more than one output should be shorted at a time.

Note 5: Quiescent I_{CC} is measured (after clearing) with 2.4V applied to all clear and A inputs, B inputs grounded, all outputs OPEN, C_{EXT} = 0.02 μF, and R_{EXT} = 25 KΩ.

Note 6: I_{CC} is measured in the triggered state with 2.4V applied to all clear and B inputs, A inputs grounded, all outputs OPEN, C_{EXT} = 0.02 μF, and R_{EXT} = 25 kΩ.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	From (Input) To (Output)	C_L = 15 pF, R_L = 400Ω C_{EXT} = 1000 pF, R_{EXT} = 10 KΩ		Units
			Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	$\overline{A}$ to Q		33	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	B to Q		28	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	$\overline{A}$ to $\overline{Q}$		40	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	B to $\overline{Q}$		36	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clear to $\overline{Q}$		40	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	$\overline{Clear}$ to Q		27	ns
$t_{WH(out)}$	Output Pulse Width (Note 7)	A or B to Q	3.08	3.76	μs

Note 7: C_{EXT} = 1000 pF, R_{EXT} = 10 kΩ