

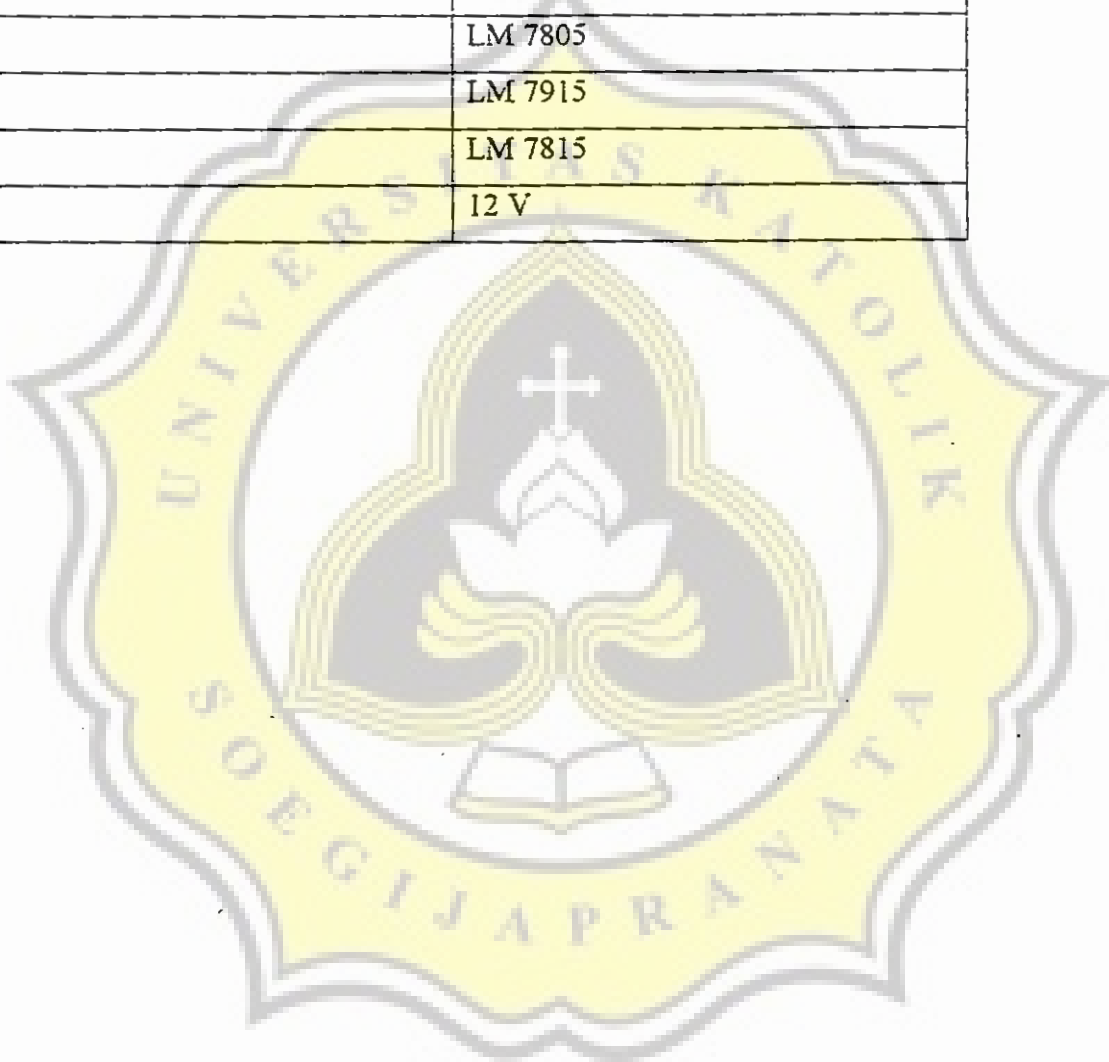
LAMPIRAN

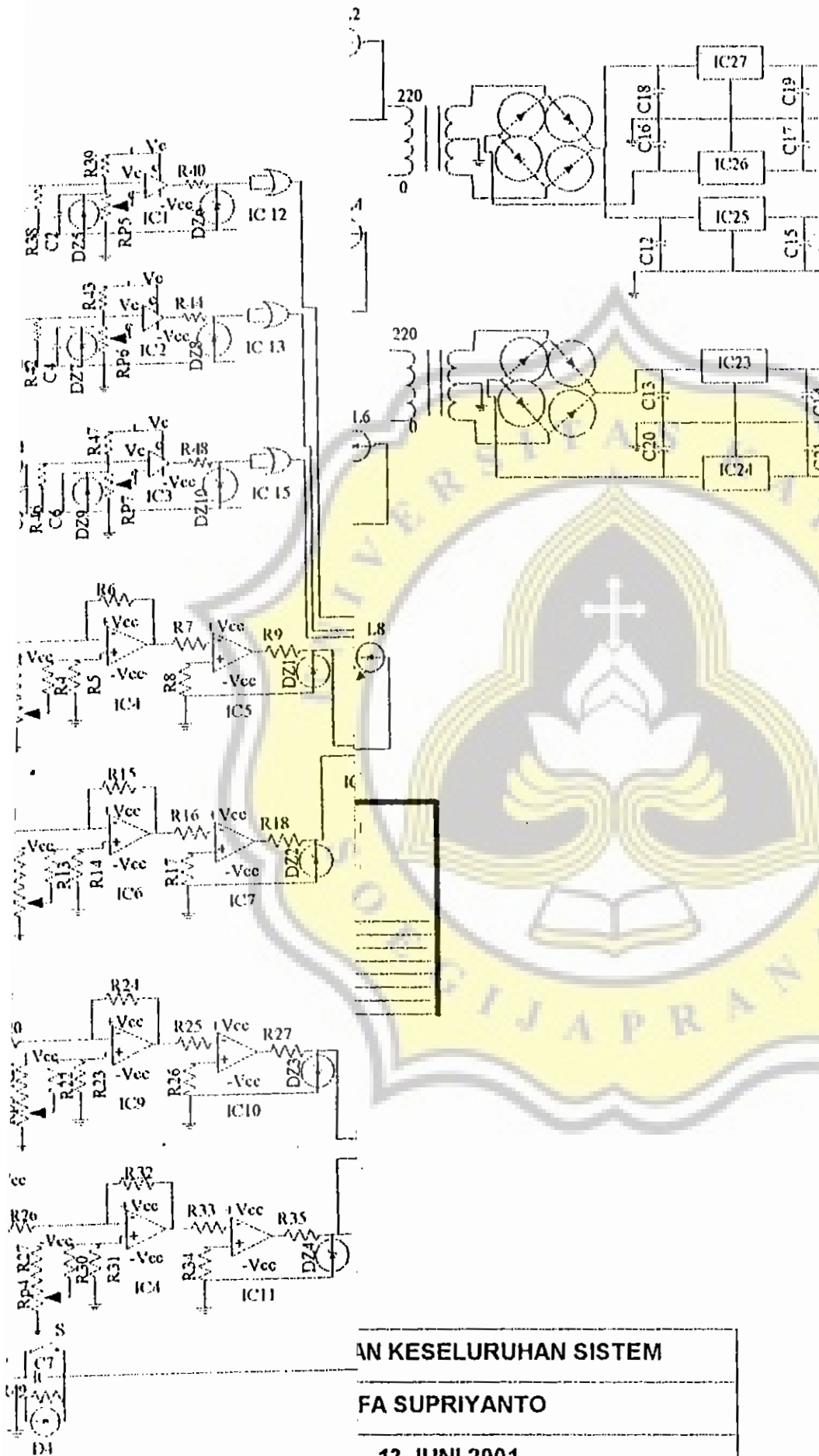


## DAFTAR KOMPONEN

Label	Nilai
R <sub>1</sub> ,R <sub>12</sub> ,R <sub>19</sub> ,R <sub>29</sub>	470 Ω
R <sub>3</sub> ,R <sub>10</sub> ,R <sub>21</sub> ,R <sub>31</sub> ,R <sub>49</sub>	1000 Ω
R <sub>18</sub> ,R <sub>26</sub> ,R <sub>36</sub>	1500 Ω
R <sub>P1-4</sub>	500 Ω
R <sub>2</sub> ,R <sub>4</sub> ,R <sub>5-8</sub> ,R <sub>11</sub> ,R <sub>13-17</sub> ,R <sub>20</sub> ,R <sub>22-22a-25</sub> ,R <sub>28</sub> ,R <sub>30</sub> ,R <sub>32</sub> 35.	2K2 Ω
R <sub>37</sub> ,R <sub>41</sub> ,R <sub>45</sub>	100 KΩ
R <sub>38</sub> ,R <sub>42</sub> ,R <sub>46</sub>	470 KΩ
R <sub>39-40</sub> ,R <sub>43-44</sub> ,R <sub>47-48</sub>	470 Ω
R <sub>P5-7</sub>	5 KΩ
R <sub>50</sub>	1K1 Ω
R <sub>51-58</sub>	20 Ω
C <sub>1</sub> ,C <sub>3</sub> ,C <sub>5</sub>	4,7 μ / 16 V
C <sub>8</sub>	10 μ / 16 V
C <sub>9-10</sub> ,C <sub>14</sub> ,C <sub>21</sub>	47 μ / 16 V
C <sub>11</sub> ,C <sub>15</sub> ,C <sub>19</sub>	470 μ / 16 V
C <sub>7</sub>	10 n
C <sub>12-13</sub> ,C <sub>16</sub> ,C <sub>18</sub> ,C <sub>20</sub>	2200 μ / 16 V
D <sub>1-12</sub>	IN 4001
DZ <sub>1-4</sub> ,DZ <sub>6</sub> ,DZ <sub>8</sub> ,DZ <sub>10</sub>	5,1 V
DZ <sub>5</sub> ,DZ <sub>7</sub> ,DZ <sub>9</sub>	12 V
TR <sub>1-8</sub>	BC 109
IC <sub>1-3</sub>	LM 084
IC <sub>4-11</sub>	LM 741
IC <sub>12-17</sub>	74LS32
IC <sub>18</sub>	74LS04

IC <sub>19</sub>	74LS00
IC <sub>20</sub>	μC 80C32
IC <sub>21</sub>	74LS373
IC <sub>22</sub>	2764K
IC <sub>23</sub>	LM 7912
IC <sub>23</sub>	LM 7912
IC <sub>24</sub>	LM 7812
IC <sub>25</sub>	LM 7805
IC <sub>26</sub>	LM 7915
IC <sub>27</sub>	LM 7815
RELAY	12 V





AN KESELURUHAN SISTEM

FA SUPRIYANTO

13 JUNI 2001

Signetics

# $\mu$ A741/ $\mu$ A741C/SA741C General Purpose Operational Amplifier

Product Specification

Linear Products

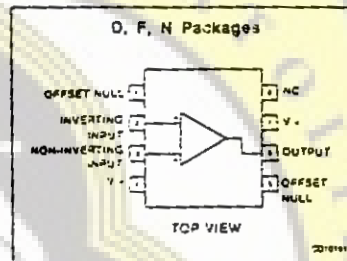
### DESCRIPTION

The  $\mu$ A741 is a high performance operational amplifier with high open-loop gain, internal compensation, high common mode range and exceptional temperature stability. The  $\mu$ A741 is short-circuit-protected and allows for nulling of offset voltage.

### FEATURES

- Internal frequency compensation
- Short circuit protection
- Excellent temperature stability
- High input voltage range

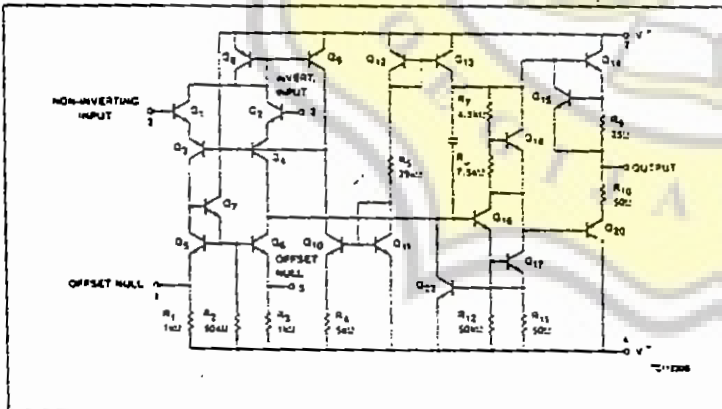
### PIN CONFIGURATION



### ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	-55°C to +125°C	$\mu$ A741N
8-Pin Plastic DIP	0 to +70°C	$\mu$ A741CN
8-Pin Plastic DIP	-40°C to +75°C	SA741CN
8-Pin Cerdip	-55°C to +125°C	$\mu$ A741F
8-Pin Cerdip	0 to +70°C	$\mu$ A741CF
8-Pin SO	0 to +70°C	$\mu$ A741CD

### EQUIVALENT SCHEMATIC



## General Purpose Operational Amplifier

 $\mu$ A741/ $\mu$ A741C/SA741C

## ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$V_S$	Supply voltage	$\pm 18$	V
	$\mu$ A741C $\mu$ A741	$\pm 22$	V
$P_D$	Internal power dissipation	500	mW
	D package	1000	mW
	N package F package	1000	mW
$V_{IN}$	Differential input voltage	$\pm 30$	V
$V_{IN}$	Input voltage <sup>1</sup>	$\pm 15$	V
$I_{SC}$	Output short-circuit duration	Continuous	
$T_A$	Operating temperature range	0 to +70	$^{\circ}$ C
	$\mu$ A741C SA741C	-40 to +85	$^{\circ}$ C
	$\mu$ A741	-55 to +125	$^{\circ}$ C
$T_{STG}$	Storage temperature range	-85 to +150	$^{\circ}$ C
$T_{SOLD}$	Lead soldering temperature (10sec max)	300	$^{\circ}$ C

## NOTE:

1. For supply voltages less than  $\pm 15V$ , the absolute maximum input voltage is equal to the supply voltage.

DC ELECTRICAL CHARACTERISTICS ( $\mu$ A741,  $\mu$ A741C)  $T_A = 25^{\circ}$ C  $V_S = \pm 15V$ , unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	$\mu$ A741			$\mu$ A741C			UNIT
			Min	Typ	Max	Min	Typ	Max	
$V_{OS}$	Offset voltage	$R_S = 10k\Omega$	1.0	5.0		2.0	5.0	mV	
$\Delta V_{OS}/\Delta T$		$R_S = 10k\Omega$ , over temp.	1.0	5.0		10	7.5	$\mu$ V/ $^{\circ}$ C	
$I_{OS}$	Offset current	Over temp.	20	200		20	200	nA	
$\Delta I_{OS}/\Delta T$		$T_A = +125^{\circ}$ C	7.0	200			300	nA	
		$T_A = -55^{\circ}$ C	20	500				nA	
			200			200		$\mu$ A/ $^{\circ}$ C	
$I_{BIAS}$	Input bias current	Over temp.	80	500		80	500	nA	
$\Delta I_B/\Delta T$		$T_A = +125^{\circ}$ C	30	500			800	nA	
		$T_A = -55^{\circ}$ C	300	1500				nA	
			1			1		nA/ $^{\circ}$ C	
$V_{OUT}$	Output voltage swing	$R_L = 10k\Omega$	$\pm 12$	$\pm 14$		$\pm 12$	$\pm 14$	V	
		$R_L = 2k\Omega$ , over temp.	$\pm 10$	$\pm 13$		$\pm 10$	$\pm 13$	V	
$A_{VOL}$	Large-signal voltage gain	$R_L = 2k\Omega$ , $V_O = \pm 10V$	50	200		20	200	V/mV	
		$R_L = 2k\Omega$ , $V_O = \pm 10V$ , over temp.	25			15		V/mV	
	Offset voltage adjustment range		$\pm 30$			$\pm 30$	mV		
PSRR	Supply voltage rejection ratio	$R_S \leq 10k\Omega$ $R_S \leq 10k\Omega$ , over temp.		10	150		10	150	$\mu$ V/V $\mu$ V/V
CMRR	Common-mode rejection ratio	Over temp.	70	90				dB dB	
$I_{CC}$	Supply current	$T_A = +125^{\circ}$ C	1.4	2.3		1.4	2.8	mA	
		$T_A = -55^{\circ}$ C	1.5	2.5				mA	
			2.0	3.3				mA	

## General Purpose Operational Amplifier

 $\mu$ A741/ $\mu$ A741C/SA741CDC ELECTRICAL CHARACTERISTICS (Continued) ( $\mu$ A741,  $\mu$ A741C)  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ , unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	$\mu$ A741			$\mu$ A741C			UNIT
			Min	Typ	Max	Min	Typ	Max	
$V_{IN}$	Input voltage range	( $\mu$ A741, over temp.)	$\pm 12$	$\pm 13$		$\pm 12$	$\pm 13$		V
$R_{IN}$	Input resistance		0.3	2.0		0.3	2.0		M $\Omega$
$P_D$	Power consumption	$T_A = +125^\circ\text{C}$ $T_A = -55^\circ\text{C}$		50 45 45	60 75 100		50	85	mW mW mW
$R_{OUT}$	Output resistance			75			75		$\Omega$
$I_{SC}$	Output short-circuit current		10	25	60	10	25	60	mA

DC ELECTRICAL CHARACTERISTICS (SA741C)  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ , unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SA741C			UNIT
			Min	Typ	Max	
$V_{OS}$	Offset voltage	$R_S = 10\text{k}\Omega$ $R_S = 10\text{k}\Omega$ , over temp.		2.0	6.0	mV
$\Delta V_{OS}/\Delta T$				10	7.5	$\mu\text{V}/^\circ\text{C}$
$I_{OS}$	Offset current	Over temp.		20	200	nA
$\Delta I_{OS}/\Delta T$				200	500	nA/ $^\circ\text{C}$
$I_{BIAS}$	Input bias current	Over temp.		90	500	nA
$\Delta I_B/\Delta T$				1	1500	nA/ $^\circ\text{C}$
$V_{OUT}$	Output voltage swing	$R_L = 10\text{k}\Omega$ $R_L = 2\text{k}\Omega$ , over temp.	$\pm 12$ $\pm 10$	$\pm 14$ $\pm 13$		V V
$A_{VOL}$	Large-signal voltage gain	$R_L = 2\text{k}\Omega$ , $V_O = \pm 10\text{V}$ $R_L = 2\text{k}\Omega$ , $V_O = \pm 10\text{V}$ , over temp.	20 15	200		V/mV V/mV
	Offset voltage adjustment range			$\pm 30$		mV
PSRR	Supply voltage rejection ratio	$R_S \leq 10\text{k}\Omega$		10	150	$\mu\text{V}/\text{V}$
$V_{IN}$	Input voltage range	( $\mu$ A741, over temp.)	$\pm 12$	$\pm 13$		V
$R_{IN}$	Input resistance		0.3	2.0		M $\Omega$
$P_D$	Power consumption			50	85	mW
$R_{OUT}$	Output resistance			75		$\Omega$
$I_{SC}$	Output short-circuit current			25		mA

AC ELECTRICAL CHARACTERISTICS  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ , unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	$\mu$ A741, $\mu$ A741C			UNIT
			Min	Typ	Max	
	Input capacitance	Open-loop, $f = 20\text{Hz}$		1.4		pF
	Crossover frequency	Open-loop		1.0		MHz
	Unity gain	$V_{IN} = 20\text{mV}$ , $R_L = 2\text{k}\Omega$ , $C_L \leq 100\text{pF}$  $C \leq 100\text{pF}$ , $R_L \geq 2\text{k}\Omega$ , $V_{IN} = \pm 10\text{V}$		0.3 5.0 0.5		$\mu\text{s}$ % V/ $\mu\text{s}$



## MCS<sup>®</sup>-51 INSTRUCTION SET

### 8051 Instruction Set Summary

Interrupt Response Time: Refer to Hardware Description Chapter.

**Instructions that Affect Flag Settings<sup>(1)</sup>**

Instruction	C	OV	AC	Instruction	C	OV	AC
ADD	X	X	X	CLR C	0		
ADDC	X	X	X	CPLC	X		
SUBB	X	X	X	ANL C, bit	X		
MUL	0	X		ANL C, /bit	X		
DIV	0	X		ORL C, bit	X		
DA	X			ORL C, /bit	X		
RRC	X			MOV C, bit	X		
RLC	X			CJNE	X		
SETB C	1						

(1) Note that operations on SFR, byte address 208 or bit addresses 209-215 (i.e., the PSW or bits in the PSW) will also affect flag settings.

**Note on instruction set and addressing modes:**

- Rn — Register R7-R0 of the currently selected Register Bank.
- direct — 8-bit internal data location's address. This could be an Internal Data RAM location (0-127) or a SFR (i.e., I/O port, control register, status register, etc. (123-255)).
- @Ri — 8-bit internal data RAM location (0-255) addressed indirectly through register Ri or R0.
- #data — 8-bit constant included in instruction.
- #data 16 — 16-bit constant included in instruction.
- addr 16 — 16-bit destination address. Used by LCALL & LJMP. A branch can be anywhere within the 64K-byte Program Memory address space.
- addr 11 — 11-bit destination address. Used by ACALL & AJMP. The branch will be within the same 2K-byte page of program memory as the first byte of the following instruction.
- rel — Signed (two's complement) 8-bit offset byte. Used by SJMP and all conditional jumps. Range is -128 to +127 bytes relative to first byte of the following instruction.
- bit — Direct Addressed bit in Internal Data RAM or Special Function Register.
- \*
- \*
- \*

\* — New operation not provided by 8048AH/8049AH.

Mnemonic	Description	Byte	Oscillator Period
<b>ARITHMETIC OPERATIONS</b>			
ADD A, Rn	Add register to Accumulator	1	12
ADD A, direct	Add direct byte to Accumulator	2	12
ADD A, @Ri	Add indirect RAM to Accumulator	1	12
ADD A, #data	Add immediate data to Accumulator	2	12
ADDC A, Rn	Add register to Accumulator with Carry	1	12
ADDC A, direct	Add direct byte to Accumulator with Carry	2	12
ADDC A, @Ri	Add indirect RAM to Accumulator with Carry	1	12
ADDC A, #data	Add immediate data to Acc with Carry	2	12
SUBB A, Rn	Subtract Register from Acc with borrow	1	12
SUBB A, direct	Subtract direct byte from Acc with borrow	2	12
SUBB A, @Ri	Subtract indirect RAM from ACC with borrow	1	12
SUBB A, #data	Subtract immediate data from Acc with borrow	2	12
INC A	Increment Accumulator	1	12
INC Rn	Increment register	1	12
INC direct	Increment direct byte	2	12
INC @Ri	Increment indirect RAM	1	12
DEC A	Decrement Accumulator	1	12
DEC Rn	Decrement Register	1	12
DEC direct	Decrement direct byte	2	12
DEC @Ri	Decrement indirect RAM	1	12





MCS-51 PROGRAMMER'S GUIDE AND INSTRUCTION SET

8051 Instruction Set Summary (Continued)

Mnemonic	Description	Byte	Oscillator Period	Mnemonic	Description	Byte	Oscillator Period
<b>ARITHMETIC OPERATIONS (Continued)</b>				<b>LOGICAL OPERATIONS (Continued)</b>			
INC DPTR	Increment Data Pointer	1	24	RL A	Rotate Accumulator Left	1	12
MUL AB	Multiply A & B	1	48	RLC A	Rotate Accumulator Left through the Carry	1	12
DIV AB	Divide A by B	1	48	RR A	Rotate Accumulator Right	1	12
DA A	Decimal Adjust Accumulator	1	12	RRC A	Rotate Accumulator Right through the Carry	1	12
<b>LOGICAL OPERATIONS</b>				<b>DATA TRANSFER</b>			
ANL A,Rn	AND Register to Accumulator	1	12	MOV A,Rn	Move register to Accumulator	1	12
ANL A,direct	AND direct byte to Accumulator	2	12	MOV A,direct	Move direct byte to Accumulator	2	12
ANL A,@Ri	AND indirect RAM to Accumulator	1	12	MOV A,@Ri	Move indirect RAM to Accumulator	1	12
ANL A,#data	AND immediate data to Accumulator	2	12	MOV A,#data	Move immediate data to Accumulator	2	12
ANL direct,A	AND Accumulator to direct byte	2	12	MOV Rn,A	Move Accumulator to register	1	12
ANL direct,#data	AND immediate data to direct byte	3	24	MOV Rn,direct	Move direct byte to register	2	24
ORL A,Rn	OR register to Accumulator	1	12	MOV Rn,#data	Move immediate data to register	2	12
ORL A,direct	OR direct byte to Accumulator	2	12	MOV direct,A	Move Accumulator to direct byte	2	12
ORL A,@Ri	OR indirect RAM to Accumulator	1	12	MOV direct,Rn	Move register to direct byte	2	24
ORL A,#data	OR immediate data to Accumulator	2	12	MOV direct,direct	Move direct byte to direct byte	3	24
ORL direct,A	OR Accumulator to direct byte	2	12	MOV direct,@Ri	Move indirect RAM to direct byte	2	24
ORL direct,#data	OR immediate data to direct byte	3	24	MOV direct,#data	Move immediate data to direct byte	3	24
XRL A,Rn	Exclusive-OR register to Accumulator	1	12	MOV @Ri,A	Move Accumulator to indirect RAM	1	12
XRL A,direct	Exclusive-OR direct byte to Accumulator	2	12				
XRL A,@Ri	Exclusive-OR indirect RAM to Accumulator	1	12				
XRL A,#data	Exclusive-OR immediate data to Accumulator	2	12				
XRL direct,A	Exclusive-OR Accumulator to direct byte	2	12				
XRL direct,#data	Exclusive-OR immediate data to direct byte	3	24				
CLR A	Clear Accumulator	1	12				
CPL A	Complement Accumulator	1	12				

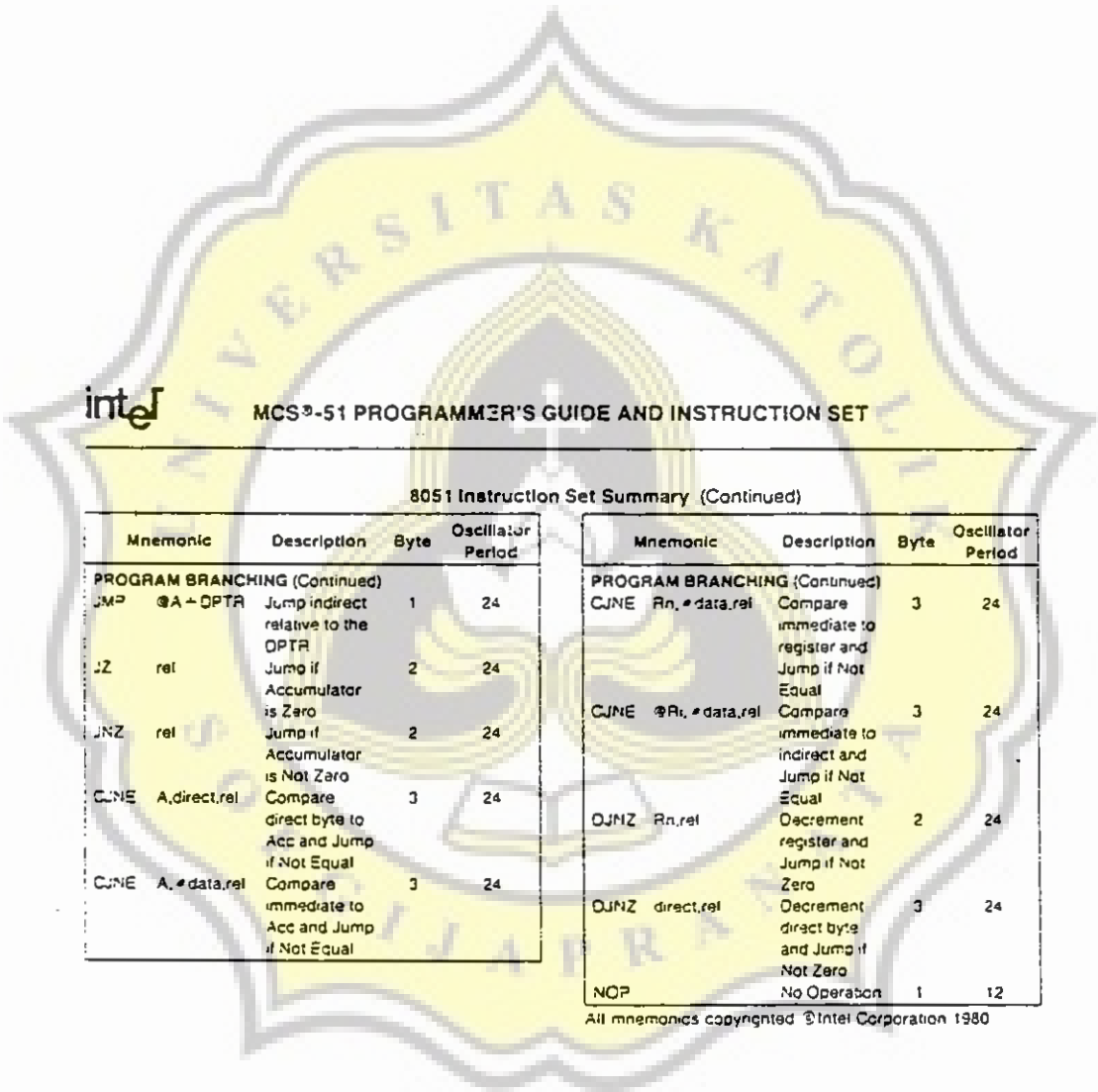
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MCS<sup>2</sup>-51 PROGRAMMER'S GUIDE AND INSTRUCTION SET

8051 Instruction Set Summary (Continued)

Mnemonic	Description	Byte	Oscillator Period	Mnemonic	Description	Byte	Oscillator Period
<b>DATA TRANSFER (Continued)</b>				<b>BOOLEAN VARIABLE MANIPULATION</b>			
MOV @Ri, direct	Move direct byte to indirect RAM	2	24	CLR C	Clear Carry	1	12
MOV @Ri, #data	Move immediate data to indirect RAM	2	12	CLR bit	Clear direct bit	2	12
MOV DPTR, #data16	Load Data Pointer with a 16-bit constant	3	24	SETB C	Set Carry	1	12
MOVC A, @A + DPTR	Move Code byte relative to DPTR to Acc	1	24	SETB bit	Set direct bit	2	12
MOVC A, @A + PC	Move Code byte relative to PC to Acc	1	24	CPL C	Complement Carry	1	12
MOVX A, @Ri	Move External RAM (8-bit addr) to Acc	1	24	CPL bit	Complement direct bit	2	12
MOVX A, @DPTR	Move External RAM (16-bit addr) to Acc	1	24	ANL C, bit	AND direct bit to CARRY	2	24
MOVX @Ri, A	Move Acc to External RAM (8-bit addr)	1	24	ANL C, /bit	AND complement of direct bit to Carry	2	24
MOVX @DPTR, A	Move Acc to External RAM (16-bit addr)	1	24	ORL C, bit	OR direct bit to Carry	2	24
PUSH direct	Push direct byte onto stack	2	24	ORL C, /bit	OR complement of direct bit to Carry	2	24
POP direct	Pop direct byte from stack	2	24	MOV C, bit	Move direct bit to Carry	2	12
XCH A, Rn	Exchange register with Accumulator	1	12	MOV bit, C	Move Carry to direct bit	2	24
XCH A, direct	Exchange direct byte with Accumulator	2	12	JC rel	Jump if Carry is set	2	24
XCH A, @Ri	Exchange indirect RAM with Accumulator	1	12	JNC rel	Jump if Carry not set	2	24
XCHD A, @Ri	Exchange low-order Digit indirect RAM with Acc	1	12	JB bit, rel	Jump if direct Bit is set	3	24
				JNB bit, rel	Jump if direct Bit is Not set	3	24
				JBC bit, rel	Jump if direct Bit is set & clear bit	3	24
				<b>PROGRAM BRANCHING</b>			
				ACALL addr11	Absolute Subroutine Call	2	24
				LCALL addr16	Long Subroutine Call	3	24
				RET	Return from Subroutine	1	24
				RETI	Return from interrupt	1	24
				AJMP addr11	Absolute jump	2	24
				LJMP addr16	Long jump	3	24
				SJMP rel	Short jump (relative addr)	2	24

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MCS<sup>®</sup>-51 PROGRAMMER'S GUIDE AND INSTRUCTION SET

8051 Instruction Set Summary (Continued)

Mnemonic	Description	Byte	Oscillator Period	Mnemonic	Description	Byte	Oscillator Period
<b>PROGRAM BRANCHING (Continued)</b>				<b>PROGRAM BRANCHING (Continued)</b>			
JMP	@A + DPTR Jump indirect relative to the DPTR	1	24	CJNE	Rn, #data,rel Compare immediate to register and Jump if Not Equal	3	24
JZ	rel Jump if Accumulator is Zero	2	24	CJNE	@Ri, #data,rel Compare immediate to indirect and Jump if Not Equal	3	24
JNZ	rel Jump if Accumulator is Not Zero	2	24	DJNZ	Rn,rel Decrement register and Jump if Not Zero	2	24
CJNE	A,direct,rel Compare direct byte to Acc and Jump if Not Equal	3	24	DJNZ	direct,rel Decrement direct byte and Jump if Not Zero	3	24
CJNE	A, #data,rel Compare immediate to Acc and Jump if Not Equal	3	24	NOP	No Operation	1	12

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