LAMPIRAN A

PROGRAM PENGENDALI PINTU KERETA API OTOMATIS

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;PROGRAM SISTEM PENGENDALI PINTU KERETA API OTOMATIS
;BERBASIS MIKROKONTROLER 80C31
;Tugas Akhir : Adi Suryanto (9350008)
;Jurusan Teknik Elektronika - FTI
;UNIVERSITAS KATOLIK SOEGIJAPRANATA SEMARANG

BUKATTUP        EQU     20H

KIRI            EQU     21H
KANAN           EQU     22H

SKIRI           EQU     P1.0
SKANAN          EQU     P1.1
SJALANA         EQU     P1.2
SJALANB         EQU     P1.3

FIN             EQU     P1.4
RIN             EQU     P1.5
SBUKA           EQU     P1.6
STUTUP          EQU     P1.7

BUKAMAN         EQU     P3.2
TUTUPMAN        EQU     P3.3

ALARM           EQU     P3.7

        ORG     00H
        LJMP    START

        ORG     03H
        LJMP    BUKA

        ORG     013H
        LJMP    TUTUP

        ORG     100H
START
        MOV     BUKATTUP,#00H
        MOV     KIRI,#00H
        MOV     KANAN,#00H
        CLR     ALARM

        MOV     IE,#85H
        SETB    IT0
        SETB    IT1

UTAMA
        JB      SKIRI,CEKKANAN
```

```
            MOV     KIRI,#01H
            AJMP    TERUS

CEKKANAN
            JB      SKANAN,KEMBALI
            MOV     KANAN,#01H
            AJMP    TERUS

KEMBALI
            AJMP    UTAMA

TERUS       SETB    ALARM

ADAMBL      JNB     SJALANA,ADAMBL
            JNB     SJALANB,ADAMBL
            SETB    RIN
            CLR     FIN
KEBAWAH     JB      STUTUP,KEBAWAH
            CLR     FIN
            CLR     RIN
            MOV     BUKATTUP,#01H

            MOV     A,KIRI
            CJNE    A,#01H,DARIKNN
TUNGGU      JB      SKANAN,TUNGGU
            MOV     KIRI,#00H
            JMP     LEWAT

DARIKNN     JB      SKIRI,DARIKNN
            MOV     KANAN,#00H

LEWAT       SETB    FIN
            CLR     RIN
KEATAS      JB      SBUKA,KEATAS
            CLR     FIN
            CLR     RIN
            MOV     BUKATTUP,#00H

            CLR     ALARM

            MOV     R4,#04H
TUNDA       MOV     R3,#0FFH
TUNDA1      MOV     R2,#0FFH
TUNDA2      NOP
            NOP
            DJNZ    R2,TUNDA2
            DJNZ    R3,TUNDA1
            DJNZ    R4,TUNDA
```

```
        JMP     UTAMA

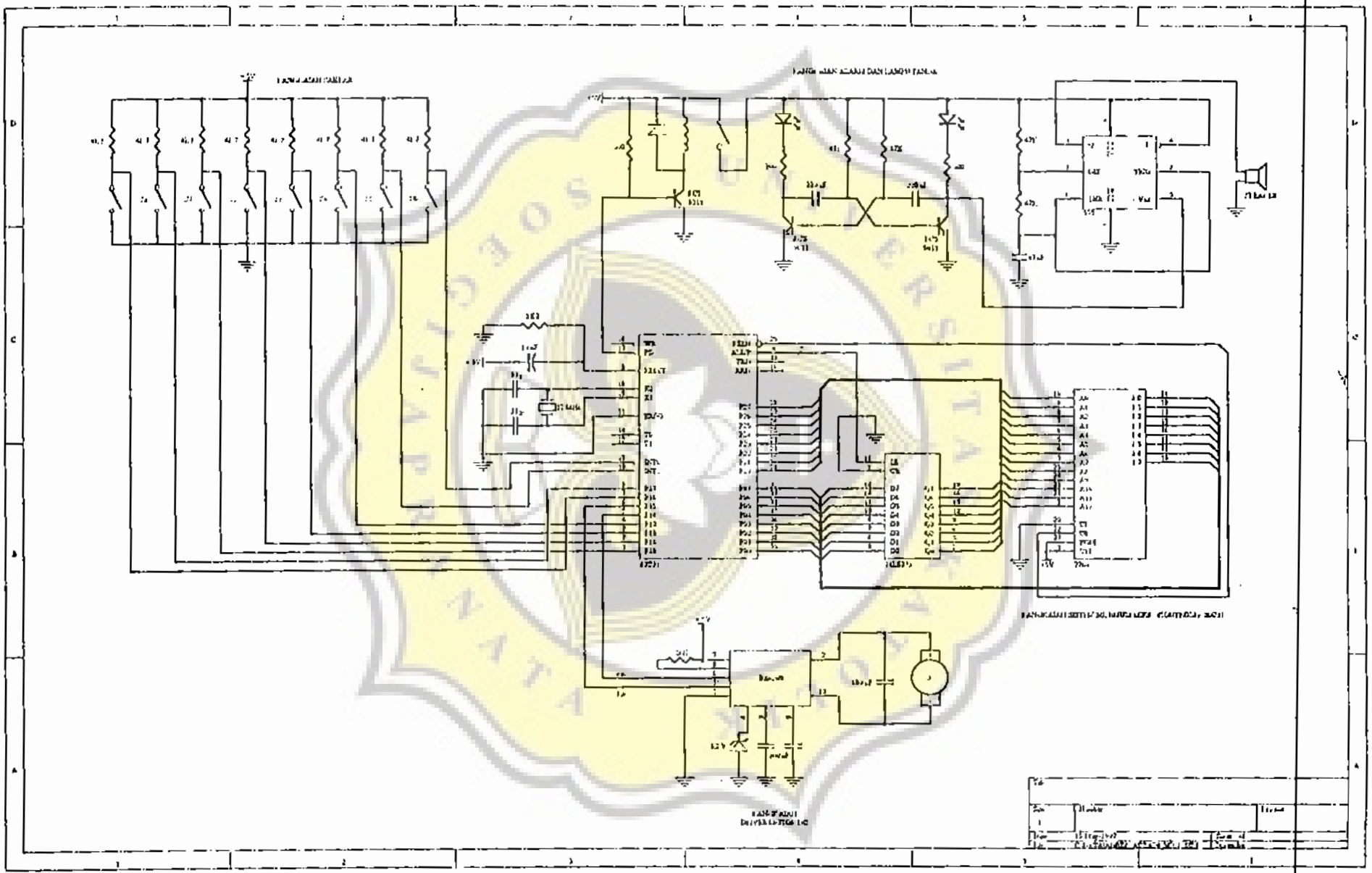
BUKA
        MOV     A,BUKATTUP
        CJNE    A,#01H,SUDAH
        SETB    FIN
        CLR     RIN
NAIK    JB      SBUKA,NAIK
        CLR     FIN
        CLR     RIN
        MOV     BUKATTUP,#00H
SUDAH   RETI

TUTUP
        MOV     A,BUKATTUP
        CJNE    A,#00H,LONCAT
        SETB    RIN
        CLR     FIN
TURUN   JB      STUTUP,TURUN
        CLR     FIN
        CLR     RIN
        MOV     BUKATTUP,#01H
LONCAT  RETI

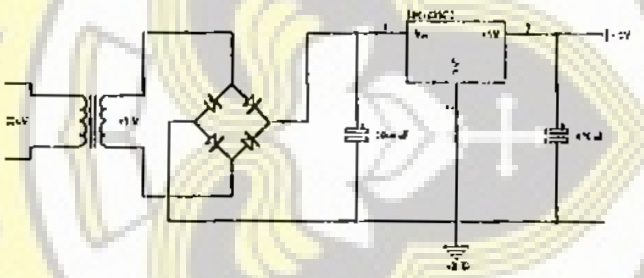
        END
```

LAMPIRAN B

GAMBAR RANGKAIAN SIESTEM MINIMUM PENGENDALI PINTU KERETA API



RANGKAIAN CATU DAYA



LAMPIRAN C
DAFTAR KOMPONEN

Daftar Komponen

NAMA KOMPONEN	HARGA	JUMLAH
1. Kapasitor	33 pF	2
	47 nF	1
	100 nF	3
	10 µ F	1
	220 µ F	2
2. Resistor	300Ω	3
	4K7Ω	6
	8K2Ω	1
	10KΩ	1
	47KΩ	4
3. Transistor	FC.9011	3
4. Dioda	0,25A	1
5. Led	-	1
6. Relay	-	1
7. Limit Switch	-	2
8. Sakelar	push on	2
9. Sakelar	push button	2

10. IC 80C31	80C31	1
11. IC 74LS373	74LS373	1
12. IC 2764	2764	1
13. IC 555	555	1
14. IC BA 6209	BA 6209	1
15. Speaker	-	1
16. Transformator	1A	1
17. Kristal	12 MHz	1

LAMPIRAN D

DATA BOOK IC BA 6209

Reversible motor driver

BA6209 / BA6209N

The BA6209 and BA6209N are reversible-motor drivers suitable for brush motors. Two logic inputs allow three output modes : forward, reverse, and braking. The motor revolving speed can be set arbitrarily by controlling the voltage applied to the motor with the control pin voltage V_R.

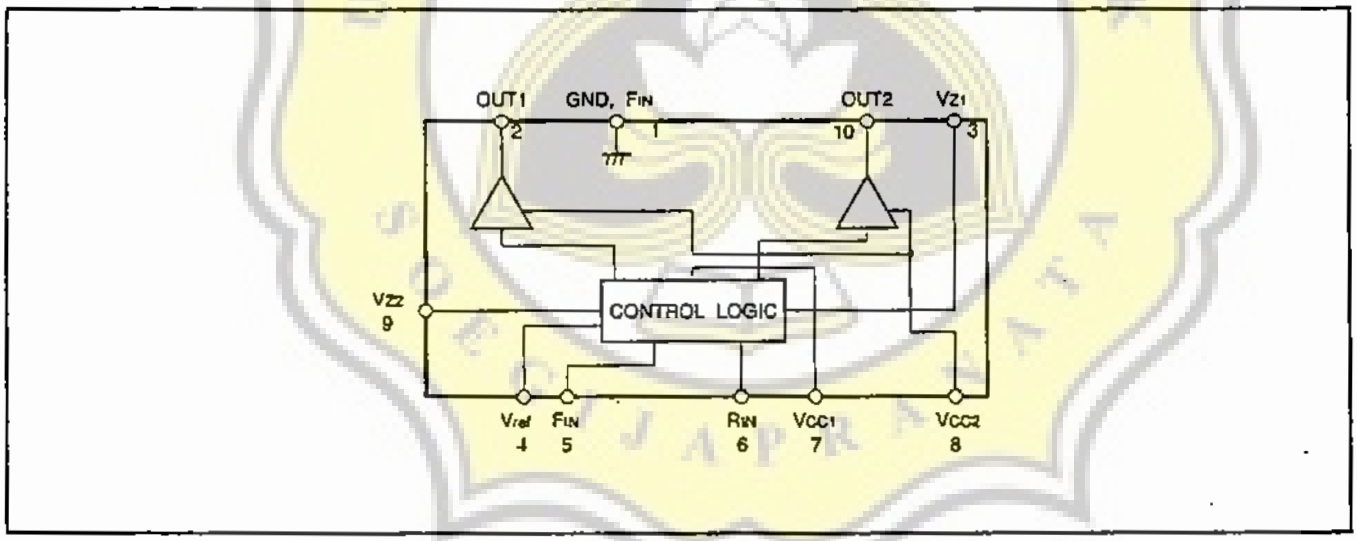
●Applications

VCRs and cassette tape recorders

●Features

1) Power transistors can handle a large current (1.6A maximally).
2) Brake is applied when stopping the motor.
3) Built-in function to absorb rush currents generated by reversing and braking.
4) Motor speed controlling pin.
5) Small standby current. (V_{CC} = 12V, I_O = 5.5mA typically)
6) Stable operation during mode changes either from forward to reverse or vice versa.
7) Interface with CMOS devices.

●Block diagram



●Absolute maximum ratings (Ta = 25°C)

Parameter		Symbol	Limits	Unit
Power supply voltage		Vcc	18	V
Power dissipation	BA6209	Pd	2200*1	mW
	BA6209N		1000*2	
Output current		Io	1.6*3	A
Input voltage		V_{IN}	−0.3~Vcc	V
Operating temperature		Topr	−20~+75	℃
Storage temperature		Tstg	−55~+125	℃

*1 Reduced by 22 mW for each increase in Ta of 1℃ over 25℃.

*2 Reduced by 10 mW for each increase in Ta of 1℃ over 25℃.

*3 500 μs pulse with a duty ratio of 1%.

●Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating voltage 1 (Logic section)	V_{CC1}	6.0	—	18.0	V
Operating voltage 2 (Output section)	V_{CC2}	—	—	18.0	V

●Electrical characteristics (unless otherwise noted, Ta = 25°C and Vcc = 12V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Current dissipation	Icc	—	5.5	10	mA	F_{IN}=R_{IN}=GND, R_L=∞
Minimum input ON current	I_{IN}	—	10	50	μA	R_L=∞
Input threshold voltage	V_{TH}	0.7	1.2	2.0	V	R_L=∞
Output leakage current	I_{OL}	—	—	1.0	mA	F_{IN}=R_{IN}=GND, R_L=∞
Output voltage	Vo	6.6	7.2	—	V	R_L=60Ω, ZD=7.4V

●Electrical characteristic curves

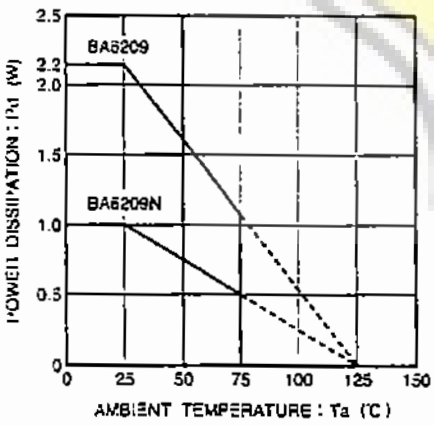


Fig.1 Temperature dependence power dissipation curves

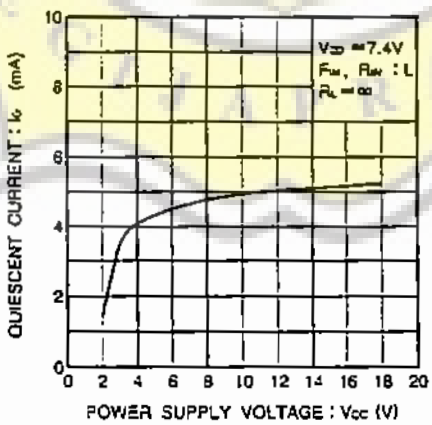


Fig.2 Quiescent current vs. power supply voltage

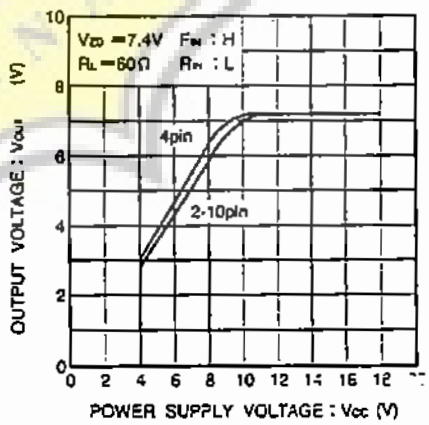


Fig.3 Maximum output voltage vs. power supply voltage (I)

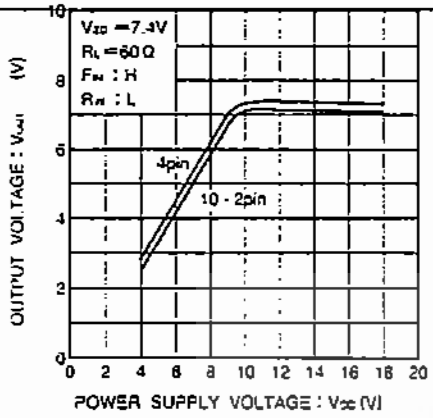


Fig.4 Maximum output voltage vs. power supply voltage (Ⅱ)

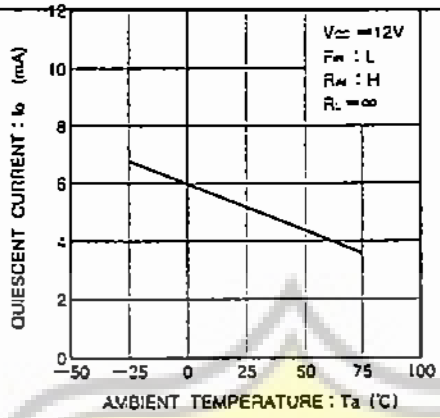


Fig.5 Quiescent current vs. ambient temperature

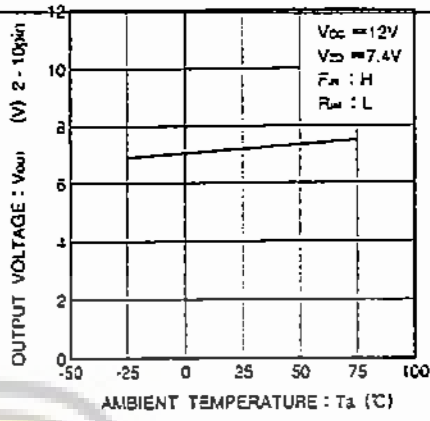


Fig.6 Output voltage vs. ambient temperature

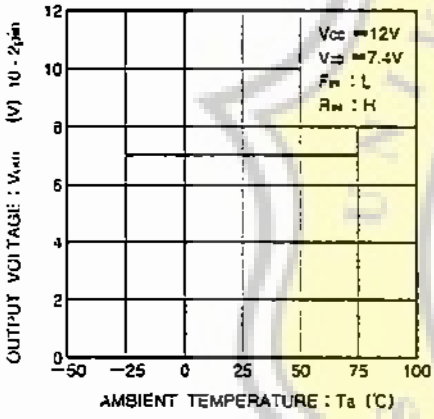


Fig.7 Output voltage vs. ambient temperature

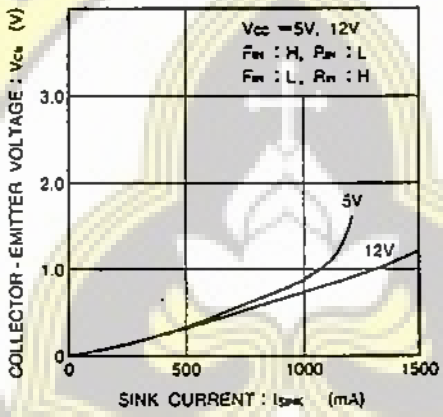


Fig.8 Output saturated voltage vs. sink current (Ⅰ)

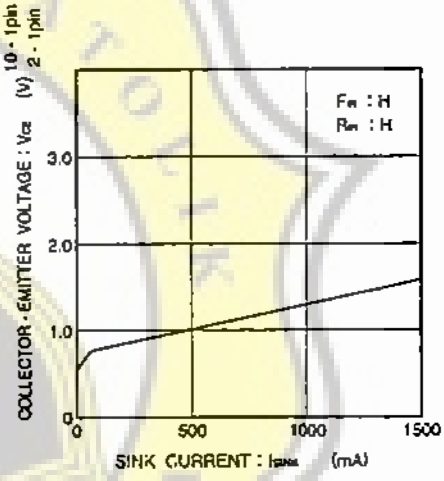


Fig.9 Output saturated voltage vs. sink current (Ⅱ)

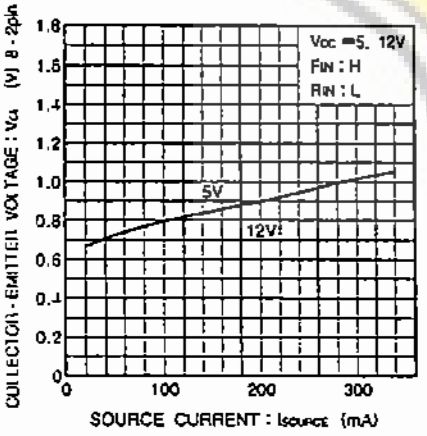


Fig.10 Output saturated voltage vs. source current (Ⅰ)

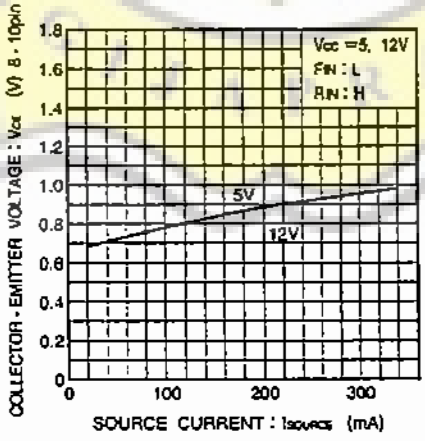


Fig.11 Output saturated voltage vs. source current (Ⅱ)

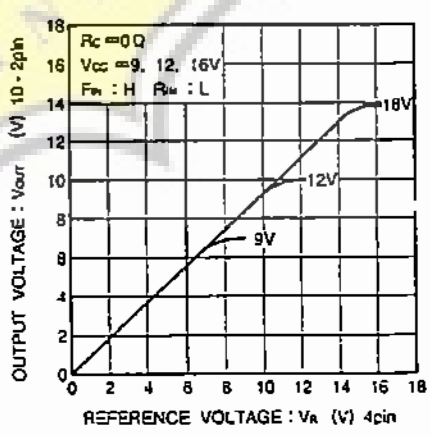


Fig.12 Output voltage vs. reference voltage (Ⅰ)

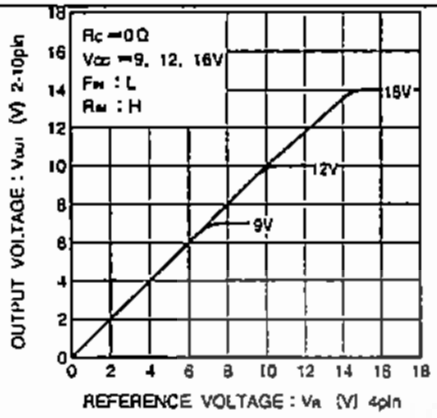


Fig.13 Output voltage vs. reference voltage (Ⅱ)

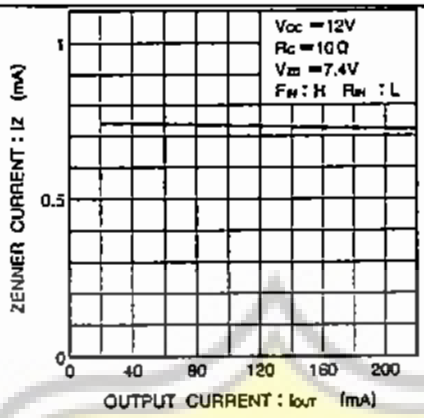


Fig.14 Zener current vs. output current

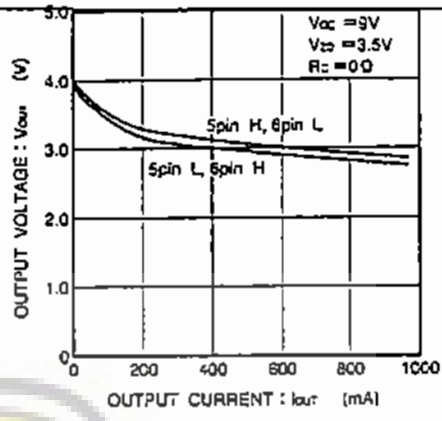


Fig.15 Output voltage vs. output current

●Measurement circuit

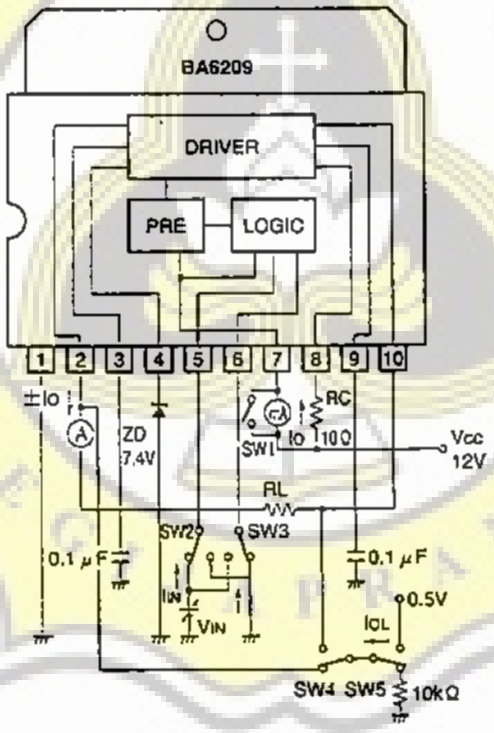


Fig.16

●Circuit operation

Input / output truth table

Input		Output	
F_{IN}	R_{IN}	OUT1	OUT2
L	L	L	L
H	L	H	L
L	H	L	H
H	H	L	L

Forward / reverse control, forced stop, and rush current absorption are controlled by the combination of F_{IN} and R_{IN} input states.

(1) Forward / reverse control circuit

When F_{IN} is HIGH and R_{IN} is LOW, current flows from OUT1 to OUT2. When F_{IN} is LOW and R_{IN} is HIGH, current flows from OUT2 to OUT1 (refer to the truth table).

(2) Forced stop circuit

By setting R_{IN} and F_{IN} both HIGH or both LOW, power supply to the motor is shut down and a brake is applied by absorbing the motor counter-electromotive force.

(3) Rush current absorption circuit

When a high voltage (caused by such as a motor reversal) is generated on OUT1 and OUT2, an internal comparator detects the high voltage and turns on an internal circuit that absorbs rush currents.

(4) Drive circuit

The forward direction of the motor connected between OUT1 and OUT2 corresponds to the current flow from OUT1 to OUT2, and the reverse direction corresponds to the current flow from OUT2 to OUT1. The output voltage (V_{OUT}) applied to the motor is given by the equation :

V_{OUT} (V) = V_{ZD} − V_{CE} (sat.) = V_{ZD} − 0.2 (I_{OUT} = 100mA)

where V_{ZD} is the zener voltage of the constant voltage diode (ZD) connected to pin 4.

If V_{ref} is left OPEN, the output voltage (V_{OUT}) is given by the equation :

V_{OUT} (V) = V_{CC1} − V_{CE} (sat.) (PNP) − 2V_F − V_{CE} (sat.)

= V_{CC1} − 1.8 (I_{OUT} = 100mA)

●Pin descriptions

Pin No.	Pin name	Function
1	GND	GND
2	OUT 1	Motor output
3	V_{Z1}	Capacitor connection pin for preventing both output transistors being turned on at the same time
4	V_{ref}	Output HIGH voltage setting
5	F_{IN}	Logic input
6	R_{IN}	Logic input
7	V_{CC1}	Control circuit power supply
8	V_{CC2}	Output power supply
9	V_{Z2}	Capacitor connection for preventing both output transistors being turned on at the same time
10	OUT 2	Motor output

●Operation notes

(1) Resistor dividing IC power consumption

To reduce power dissipated in the IC, a resistance (about 3~10Ω) must always be connected between Vcc and the power supply pin of the driver circuit. If Vcc2 is connected to Vcc with no resistor, the IC can be damaged by over-current when operated at the voltage range close to the maximum operating voltage.

(2) Control signal waveform

The rise and fall times of signals applied to the control pins should be 5ms or less. Longer times can cause erratic operation of the internal logic circuits and may result in damage to the driver circuits.

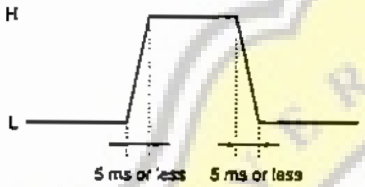


Fig.17 Control signal

For example, if the supply voltage for the external control circuit comes up after the supply voltage of the IC, the rising edge of the control signal slowly follows the rise of the external supply voltage. This could result in erratic operation or damage to the IC due to excess currents.

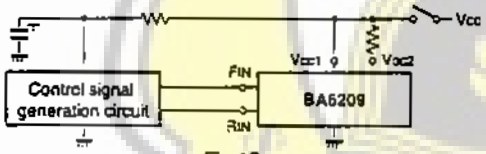


Fig.18

(3) IC ground voltage

To provide separation between the circuit elements within the IC, the GND pin of the IC must always be held at a lower potential than the other pins.

If the potential of the GND pin is allowed to rise above that of other pins (such as the control input pins), separation between the internal circuit elements could break down, resulting in erratic operation or internal damage.

For example, a resistor may be connected between GND (pin 1) and the ground as shown in Fig. 19, when detecting and controlling the motor operating current. In this case, the potential of pin 1 would be above the ground potential by an amount equal to the voltage drop across the resistor. Therefore, dropping the input pin potential to the ground potential would have the effect of applying a negative voltage to the input pin.

This should be avoided by detecting the motor operating current in a way shown in Fig. 20.

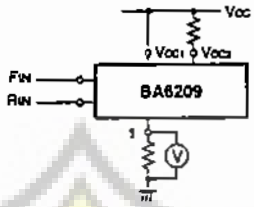


Fig.19

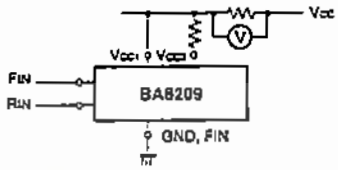


Fig.20

(4) Input pins

Voltage should never be applied to the input pins when the Vcc voltage is not applied to the IC. Similarly, when Vcc is applied, the voltage on each input pin should be less than Vcc and within the guaranteed range for the electrical characteristics.

(5) Back-rush voltage

Depending on the ambient conditions, environment, or motor characteristics, the back-rush voltage may fluctuate. Be sure to confirm that the back-rush voltage will not adversely affect the operation of the IC.

(6) Large current line

Large currents are carried by the motor power supply and motor ground for these ICs.

Therefore, the layout of the pattern of the PC board and the constants of certain parameters for external components, such as the capacitor between the power supply and ground, may cause this large output current to flow back to the input pins, resulting in output oscillation or other malfunctions. To prevent this, make sure that the PC board layout and external circuit constants cause no problems with the characteristics of these ICs.

(7) Power dissipation

The power dissipation will fluctuate depending on the mounting conditions of the IC and the ambient environment. Make sure to carefully check the thermal design of the application where these ICs sill be used.

(8) Power consumption

The power consumption by the IC varies widely with the power supply voltage and the output current. Give full consideration to the power dissipation rating and the thermal resistance data and transient thermal resistance data, to provide a thermal design so that none of the ratings for the IC are exceeded.

(9) ASO
Make sure that the output current and supply voltage do not exceed the ASO values.
(10) Precautions for input mode switching
To ensure reliability, it is recommended that the mode switching for the motor pass once through the open mode.
(11) There are no circuits built into these ICs that prevent in-rush currents. Therefore, it is recommended to place a current limiting resistor or other physical countermeasure.
(12) If the potential of the output pin sways greatly and goes below the potential of ground, the operation of the IC may malfunction or be adversely affected. In such a case, place a diode between the output and ground, or other measure, to prevent this.
(13) The quality of these products have been carefully checked; however, use of the products with applied voltages, operating temperatures, or other parameters that exceed the absolute maximum rating given may result in the damage of the IC and the product it is used in. If the IC is damaged, the short mode and open modes cannot be specified, so if the IC is to be used in applications where parameters may exceed the absolute maximum ratings, then be sure to incorporate fuses, or other physical safety measures.

●Application example

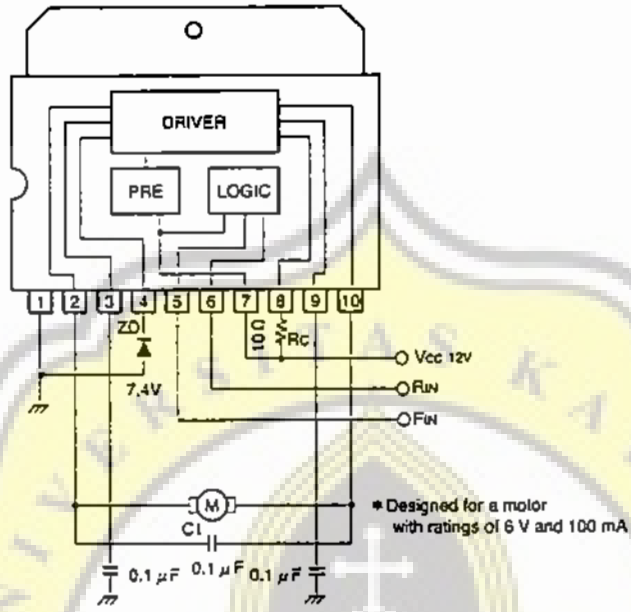
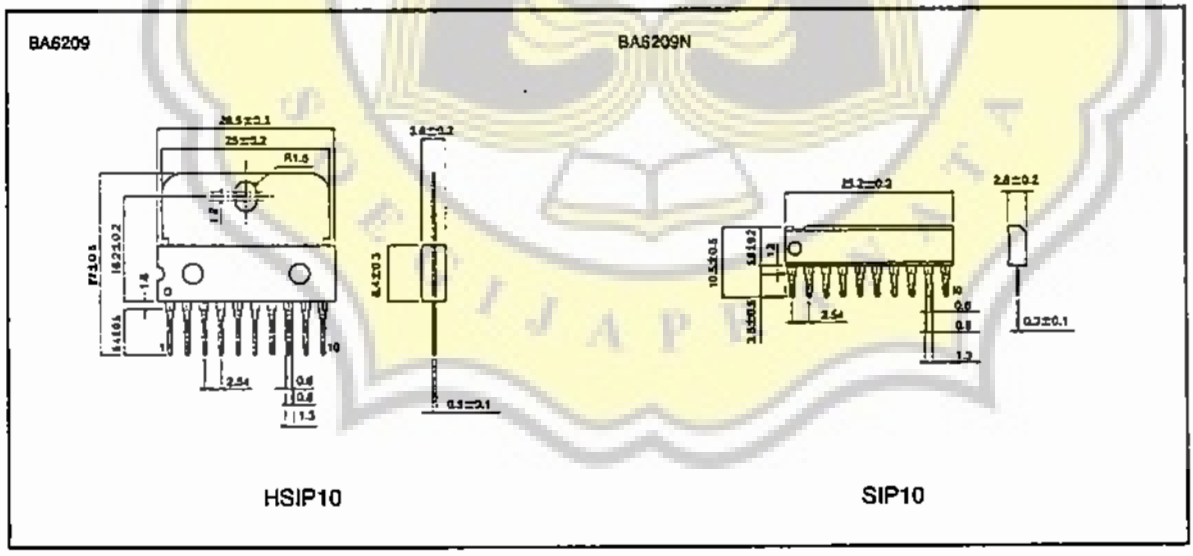


Fig.21

●External dimensions (Units: mm)



LAMPIRAN E

DATA BOOK IC 80C31

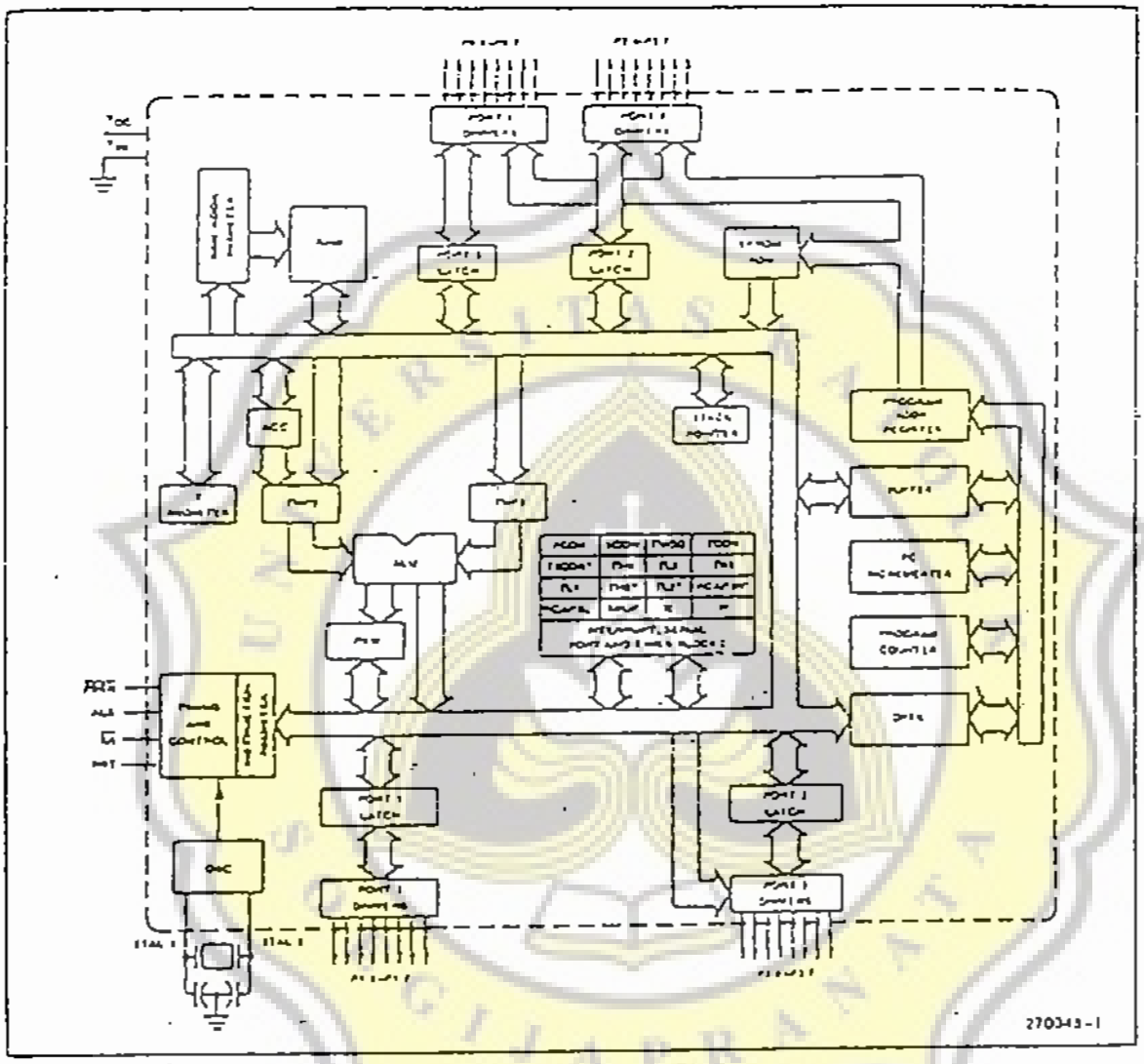


Figure 1. MCS®-51 Block Diagram

PACKAGES

Part	Prefix	Package Type
8051AH/ 8031AH	P	40-Pin Plastic DIP
	D	40-Pin CERDIP
	N	44-Pin PLCC
8052AH/ 8032AH	P	40-Pin Plastic DIP
	D	40-Pin CERDIP
	N	44-Pin PLCC
8751H/ 8751H-8	D	40-Pin CERDIP

PIN DESCRIPTIONS

V_{CC}: Supply voltage.

V_{SS}: Circuit ground.

Port 0: Port 0 is an 8-bit open drain bidirectional I/O port. As an output port each pin can sink 8 LS TTL inputs.

Port 0 pins that have 1s written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1s and can source and sink 8 LS TTL inputs.

Port 0 also receives the code bytes during programming of the EPROM parts, and outputs the code bytes during program verification of the ROM and EPROM parts. External pullups are required during program verification.

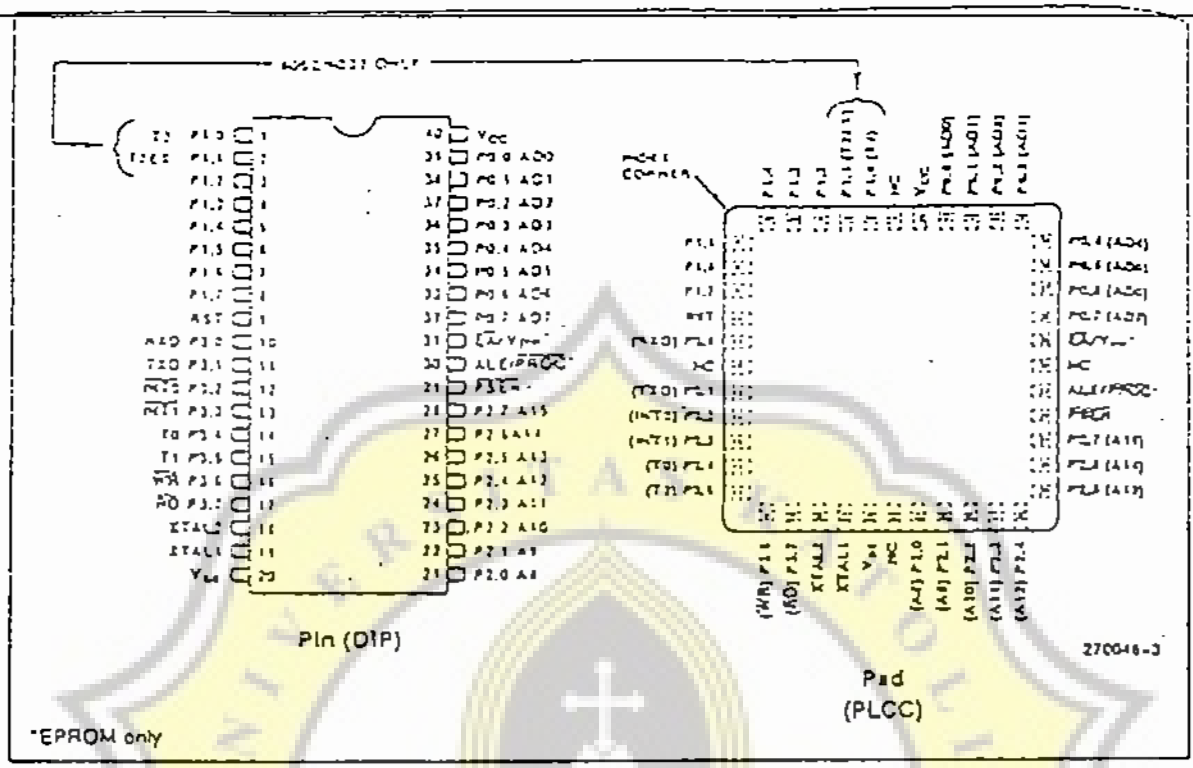


Figure 2. MCS®-51 Connections

Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source 4 LS TTL inputs. Port 1 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL} on the data sheet) because of the internal pullups.

Port 1 also receives the low-order address bytes during programming of the EPROM parts and during program verification of the ROM and EPROM parts.

In the 8032AH and 8052AH, Port 1 pins P1.0 and P1.1 also serve the T2 and T2EX functions, respectively.

Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source 4 LS TTL inputs. Port 2 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL} on the data sheet) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1s. During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits during programming of the EPROM parts and during program verification of the ROM and EPROM parts.

Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source 4 LS TTL inputs. Port 3 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL} on the data sheet) because of the pullups.

Port 3 also serves the functions of various special features of the MCS-51 Family, as listed below:

Port Pin	Alternative Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST: Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{PROG}$: Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during programming of the EPROM parts.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

$\overline{PSEN}$: Program Store Enable is the read strobe to external Program Memory.

When the device is executing code from external Program Memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external Data Memory.

$\overline{EA}$/V_{PP}: External Access enable $\overline{EA}$ must be strapped to V_{SS} in order to enable any MCS-51 device to fetch code from external Program memory locations starting at 0000H up to FFFFH. $\overline{EA}$ must be strapped to V_{CC} for internal program execution.

Note, however, that if the Security Bit in the EPROM devices is programmed, the device will not fetch code from any location in external Program Memory.

This pin also receives the 21V programming supply voltage (VPP) during programming of the EPROM parts.

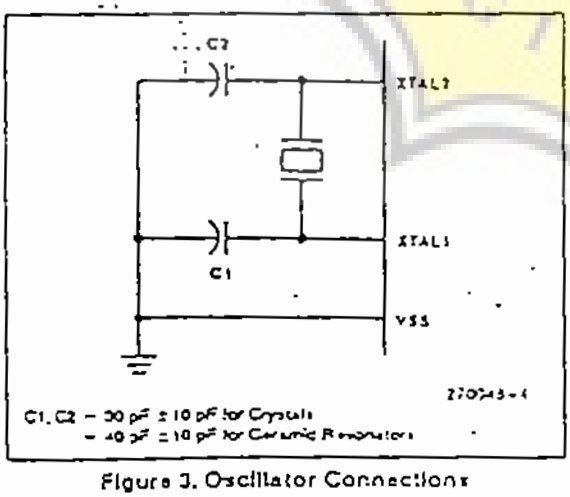


Figure 3. Oscillator Connections

XTAL1: Input to the inverting oscillator amplifier.

XTAL2: Output from the inverting oscillator amplifier.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3. Either a quartz crystal or ceramic resonator may be used. More detailed information concerning the use of the on-chip oscillator is available in Application Note AP-155, "Oscillators for Microcontrollers."

To drive the device from an external clock source, XTAL1 should be grounded, while XTAL2 is driven, as shown in Figure 4. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the Data Sheet must be observed.

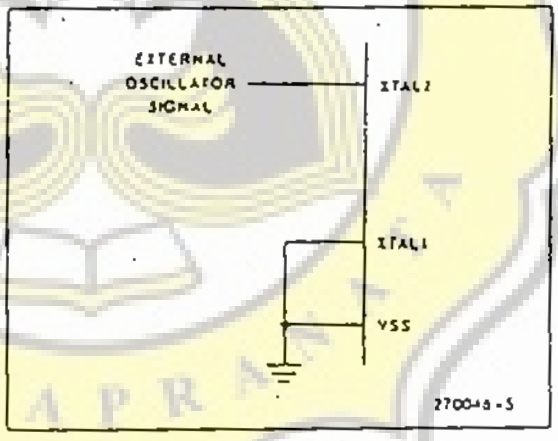


Figure 4. External Drive Configuration

DESIGN CONSIDERATIONS

If an 87518H or 87528H may replace an 8751H in a future design, the user should carefully compare both data sheets for DC or AC Characteristic differences. Note that the V_{IH} and I_{IH} specifications for the $\overline{EA}$ pin differ significantly between the devices.

Exposure to light when the EPROM device is in operation may cause logic errors. For this reason, it is suggested that an opaque label be placed over the window when the die is exposed to ambient light.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias .....0°C to 70°C
Storage Temperature .....−65°C to + 150°C
Voltage on $\overline{EA}$/V_{PP} Pin to V_{SS} ....−0.5V to + 21.5V
Voltage on Any Other Pin to V_{SS} ....−0.5V to + 7V
Power Dissipation.....1.5W

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

*WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

Operating Conditions: T_A (Under Bias) = 0°C to + 70°C; V_{CC} = 5V ± 10%; V_{SS} = 0V

D.C. CHARACTERISTICS (Under Operating Conditions)

Symbol	Parameter		Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (Except $\overline{EA}$ Pin of 8751H & 8751H-8)		−0.5	0.8	V	
V_{IL1}	Input Low Voltage to $\overline{EA}$ Pin of 8751H & 8751H-8		0	0.7	V	
V_{IH}	Input High Voltage (Except XTAL2, RST)		2.0	V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage to XTAL2, RST		2.5	V_{CC} + 0.5	V	XTAL1 = V_{SS}
V_{OL}	Output Low Voltage (Ports 1, 2, 3)*			0.45	V	I_{OL} = 1.6 mA
V_{OL1}	Output Low Voltage (Port 0, ALE, $\overline{PSEN}$)*					
		8751H, 8751H-8		0.60 0.45	V V	I_{OL} = 3.2 mA I_{OL} = 2.4 mA
		All Others		0.45	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage (Ports 1, 2, 3, ALE, $\overline{PSEN}$)		2.4		V	I_{OH} = −80 µA
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)		2.4		V	I_{OH} = −400 µA
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3, RST) 8032AH, 8052AH All Others			−800 −500	µA µA	V_{IN} = 0.45V V_{IN} = 0.45V
I_{IL1}	Logical 0 Input Current to $\overline{EA}$ Pin of 8751H & 8751H-8 Only			−15	mA	V_{IN} = 0.45V
I_{IL2}	Logical 0 Input Current (XTAL2)			−3.2	mA	V_{IN} = 0.45V
I_{LI}	Input Leakage Current (Port 0) 8751H & 8751H-8 All Others			 ±100 ±10	 µA µA	 0.45 ≤ V_{IN} ≤ V_{CC} 0.45 ≤ V_{IN} ≤ V_{CC}
I_{IH}	Logical 1 Input Current to $\overline{EA}$ Pin of 8751H & 8751H-8			500	µA	V_{IN} = 2.4V
I_{IH1}	Input Current to RST to Activate Reset			500	µA	V_{IN} < (V_{CC} − 1.5V)
I_{CC}	Power Supply Current: 8031/8051 8031AH/8051AH 8032AH/8052AH 8751H/8751H-8			 160 125 175 250	 mA mA mA mA	 All Outputs Disconnected; $\overline{EA}$ = V_{CC}
C_{IO}	Pin Capacitance			10	pF	Test freq = 1 MHz

*NOTE:
Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL}s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE line may exceed 0.8V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.

A.C. CHARACTERISTICS Under Operating Conditions:

Load Capacitance for Port 0, ALE, and $\overline{PSEN}$ = 100 pF;
Load Capacitance for All Other Outputs = 80 pF

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
1/TCLCL	Oscillator Frequency			3.5	12.0	MHz
TLHLL	ALE Pulse Width	127		2TCLCL − 40		ns
TAVLL	Address Valid to ALE Low	43		TCLCL − 40		ns
TLLAX	Address Hold after ALE Low	48		TCLCL − 35		ns
TLLIV	ALE Low to Valid Instr In 8751H All Others		 183 233		 4TCLCL − 150 4TCLCL − 100	 ns ns
TLLPL	ALE Low to $\overline{PSEN}$ Low	58		TCLCL − 25		ns
TPLPH	$\overline{PSEN}$ Pulse Width 8751H All Others	 190 215		 3TCLCL − 60 3TCLCL − 35		 ns ns
TPLIV	$\overline{PSEN}$ Low to Valid Instr In 8751H All Others		 100 125		 3TCLCL − 150 3TCLCL − 125	 ns ns
TPXIX	Input Instr Hold after $\overline{PSEN}$	0		0		ns
TPXIZ	Input Instr Float after $\overline{PSEN}$		63		TCLCL − 20	ns
TPXAV	$\overline{PSEN}$ to Address Valid	75		TCLCL − 8		ns
TAVIV	Address to Valid Instr In 8751H All Others		 287 302		 5TCLCL − 150 5TCLCL − 115	 ns ns
TPLAZ	$\overline{PSEN}$ Low to Address Float		20		20	ns
TRLRH	$\overline{RD}$ Pulse Width	400		6TCLCL − 100		ns
TWLWH	$\overline{WR}$ Pulse Width	400		6TCLCL − 100		ns
TRLDV	$\overline{RD}$ Low to Valid Data In		252		5TCLCL − 165	ns
TRHDX	Data Hold after $\overline{RD}$	0		0		ns
TRHDZ	Data Float after $\overline{RD}$		97		2TCLCL − 70	ns
TLLDV	ALE Low to Valid Data In		517		8TCLCL − 150	ns
TAVDV	Address to Valid Data In		585		9TCLCL − 165	ns
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	3TCLCL − 50	3TCLCL + 50	ns
TAVWL	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		4TCLCL − 130		ns
TQVWX	Data Valid to $\overline{WR}$ Transition 8751H All Others	 13 23		 TCLCL − 70 TCLCL − 60		 ns ns
TQVWH	Data Valid to $\overline{WR}$ High	433		7TCLCL − 150		ns
TWHQX	Data Hold after $\overline{WR}$	33		TCLCL − 50		ns
TRLAZ	$\overline{RD}$ Low to Address Float		20		20	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High 8751H All Others	 33 43	 133 123	 TCLCL − 50 TCLCL − 40	 TCLCL + 50 TCLCL + 40	 ns ns

NOTE:
*This table does not include the 8751-8 A.C. characteristics (see next page).

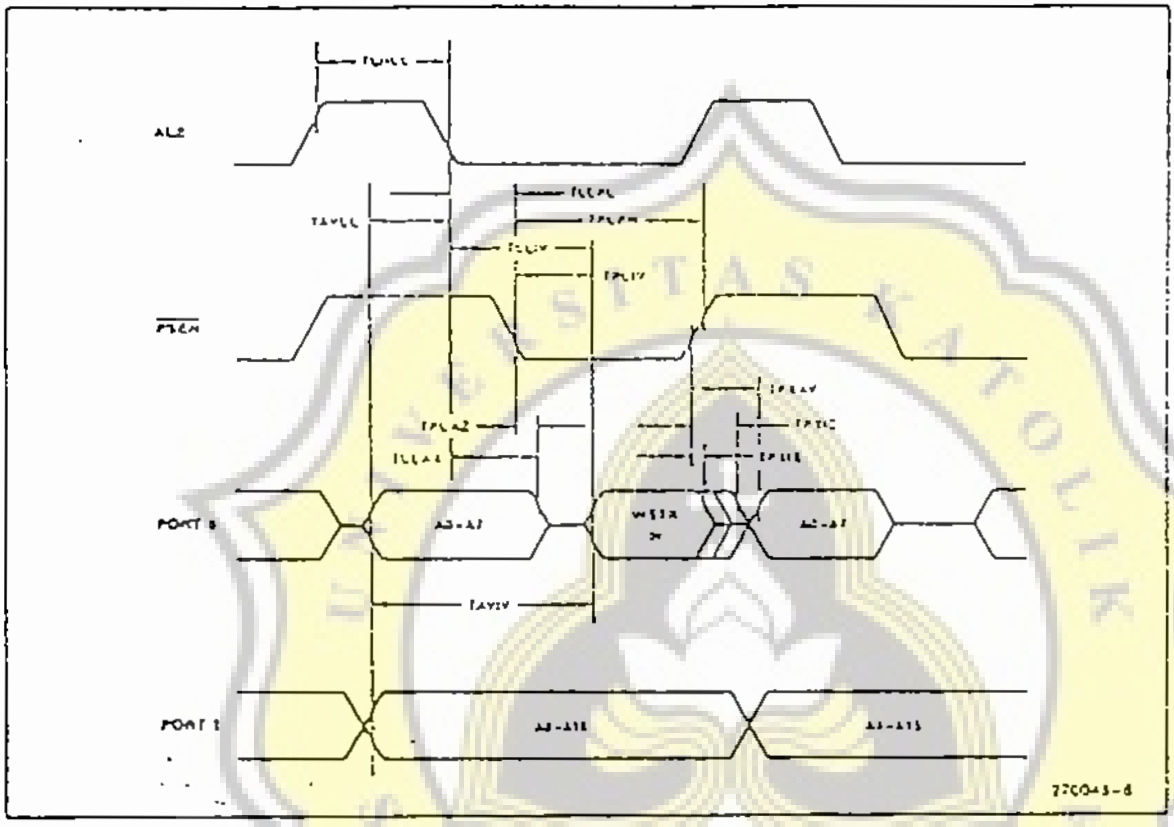
This Table is only for the 8751H-8

A.C. CHARACTERISTICS Under Operating Conditions:

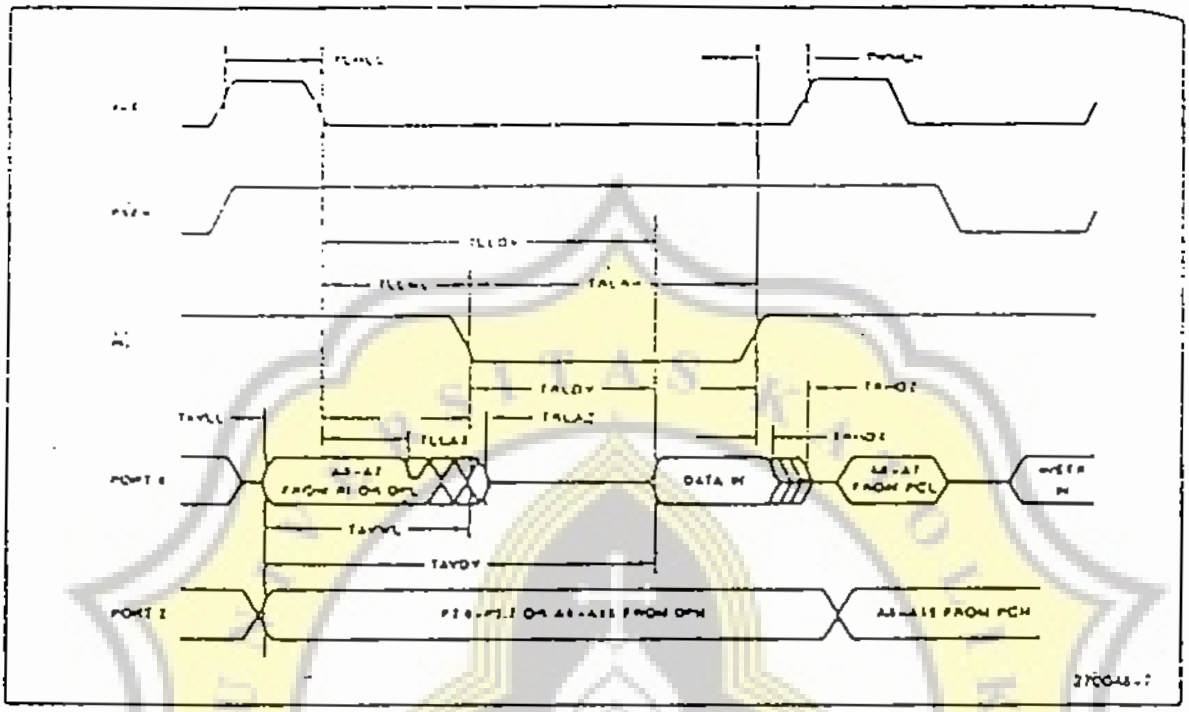
Load Capacitance for Port 0, ALE, and $\overline{PSEN}$ = 100 pF;
Load Capacitance for All Other Outputs = 80 pF

Symbol	Parameter	8 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
1/TCLCL	Oscillator Frequency			3.5	8.0	MHz
TLHLL	ALE Pulse Width	210		2TCLCL – 40		ns
TAVLL	Address Valid to ALE Low	85		TCLCL – 40		ns
TLLAX	Address Hold after ALE Low	90		TCLCL – 35		ns
TLLIV	ALE Low to Valid Instr In		350		4TCLCL – 150	ns
TLLPL	ALE Low to $\overline{PSEN}$ Low	100		TCLCL – 25		ns
TPLPH	$\overline{PSEN}$ Pulse Width	315		3TCLCL – 60		ns
TPLIV	$\overline{PSEN}$ Low to Valid Instr In		225		3TCLCL – 150	ns
TPXIX	Input Instr Hold after $\overline{PSEN}$	0		0		ns
TPXIZ	Input Instr Float after $\overline{PSEN}$		105		TCLCL – 20	ns
TPXAV	$\overline{PSEN}$ to Address Valid	117		TCLCL – 8		ns
TAVIV	Address to Valid Instr In		475		5TCLCL – 150	ns
TPLAZ	$\overline{PSEN}$ Low to Address Float		20		20	ns
TRLRH	$\overline{RD}$ Pulse Width	650		6TCLCL – 100		ns
TWLWH	$\overline{WR}$ Pulse Width	650		6TCLCL – 100		ns
TRLDV	$\overline{RD}$ Low to Valid Data In		460		5TCLCL – 165	ns
TRHDX	Data Hold after $\overline{RD}$	0		0		ns
TRHDZ	Data Float after $\overline{RD}$		180		2TCLCL – 70	ns
TLLDV	ALE Low to Valid Data In		850		8TCLCL – 150	ns
TAVDV	Address to Valid Data In		960		9TCLCL – 165	ns
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	325	425	3TCLCL – 50	3TCLCL + 50	ns
TAVWL	Address to $\overline{RD}$ or $\overline{WR}$ Low	370		4TCLCL – 130		ns
TQVWX	Data Valid to $\overline{WR}$ Transition	55		TCLCL – 70		ns
TQVWH	Data Valid to $\overline{WR}$ High	725		7TCLCL – 150		ns
TWHQX	Data Hold after $\overline{WR}$	75		TCLCL – 50		ns
TRLAZ	$\overline{RD}$ Low to Address Float		20		20	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	75	175	TCLCL – 50	TCLCL + 50	ns

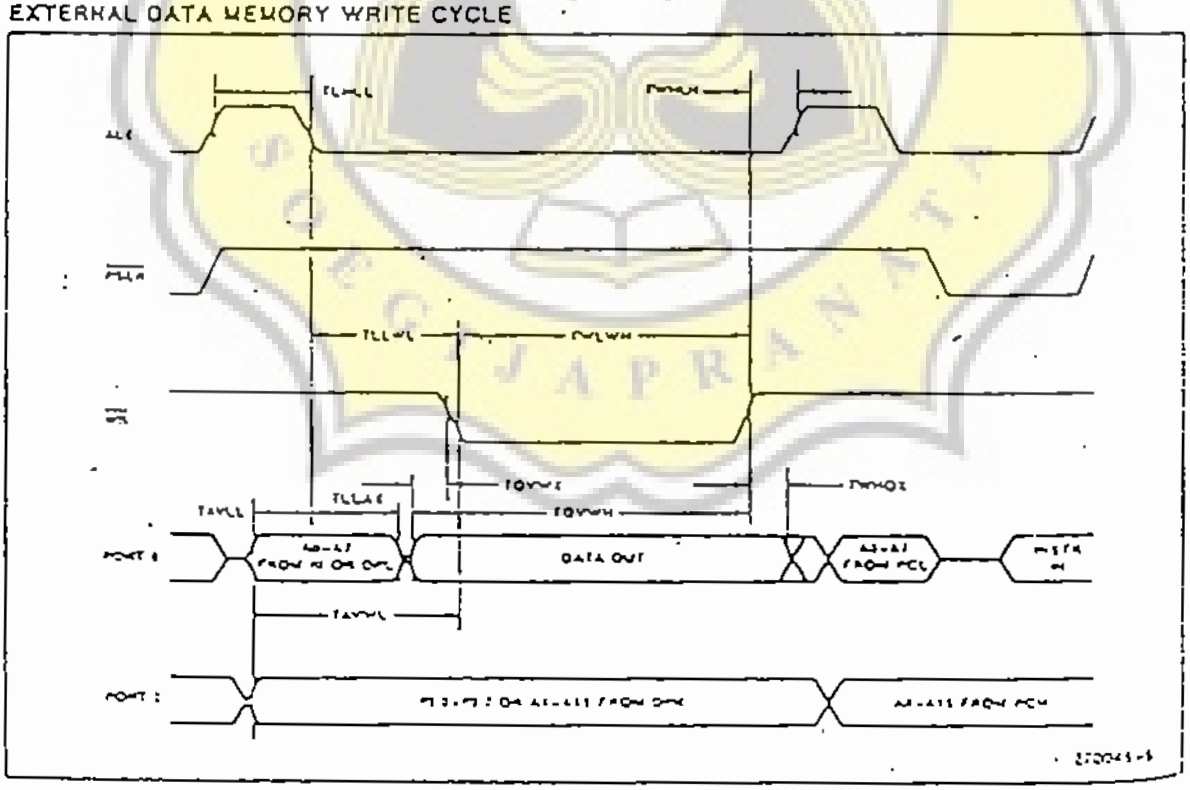
EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE



EXTERNAL DATA MEMORY WRITE CYCLE

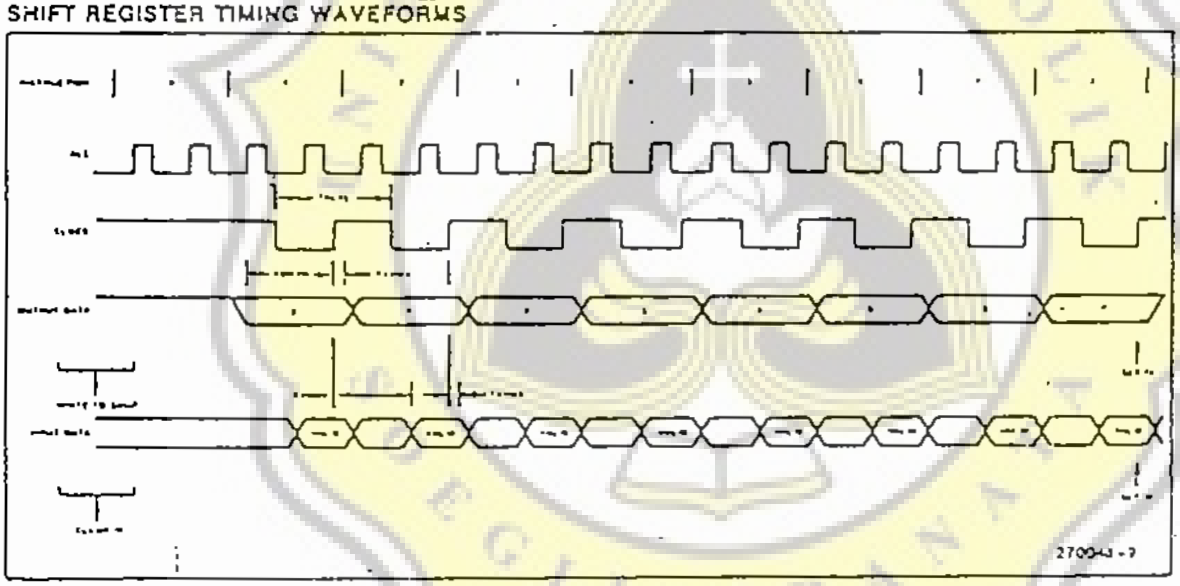


SERIAL PORT TIMING—SHIFT REGISTER MODE

Test Conditions: T_A = 0°C to 70°C; VCC = 5V ±10%; VSS = 0V; Load Capacitance = 80 pF

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	1.0		12TCLCL		µs
TQVXH	Output Data Setup to Clock Rising Edge	700		10TCLCL – 133		ns
TXHQX	Output Data Hold after Clock Rising Edge	50		2TCLCL – 117		ns
TXHDX	Input Data Hold after Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		700		10TCLCL – 133	ns

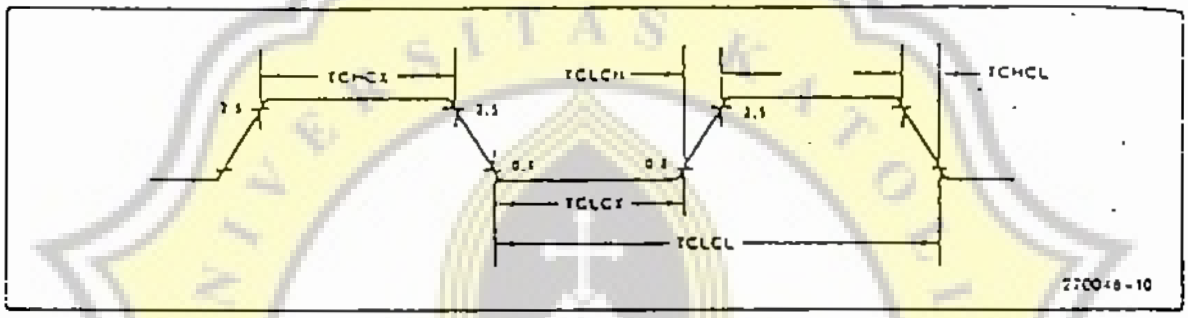
SHIFT REGISTER TIMING WAVEFORMS



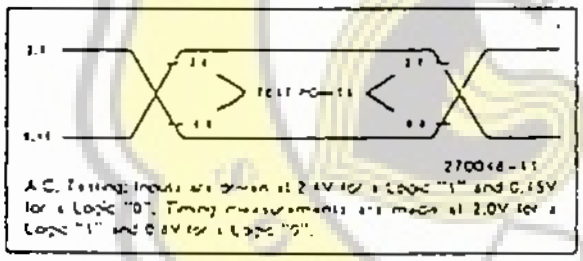
EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency (except 8751H-8) 8751H-8	3.5 3.5	12 8	MHz MHz
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

EXTERNAL CLOCK DRIVE WAVEFORM



A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. Testing: Inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

EPROM CHARACTERISTICS

Table 3. EPROM Programming Modes

Mode	RST	PSEN	ALE	EA	P2.7	P2.6	P2.5	P2.4
Program	1	0	0*	VPP	1	0	X	X
Inhibit	1	0	1	X	1	0	X	X
Verify	1	0	1	1	0	0	X	X
Security Set	1	0	0*	VPP	1	1	X	X

NOTE:
"1" = logic high for that pin
"0" = logic low for that pin
"X" = "don't care"

"VPP" = +21V ±0.5V
*ALE is pulsed low for 50 ms.

Programming the EPROM

To be programmed, the part must be running with a 4 to 6 MHz oscillator. (The reason the oscillator needs to be running is that the internal bus is being used to transfer address and program data to appropriate internal registers.) The address of an EPROM location to be programmed is applied to Port 1 and pins P2.0–P2.3 of Port 2, while the code byte to be programmed into that location is applied to Port 0. The other Port 2 pins, and RST, PSEN, and EA should be held at the "Program" levels indicated in Table 3. ALE is pulsed low for 50 ms to program the code byte into the addressed EPROM location. The setup is shown in Figure 5.

Normally EA is held at a logic high until just before ALE is to be pulsed. Then EA is raised to +21V, ALE is pulsed, and then EA is returned to a logic high. Waveforms and detailed timing specifications are shown in later sections of this data sheet.

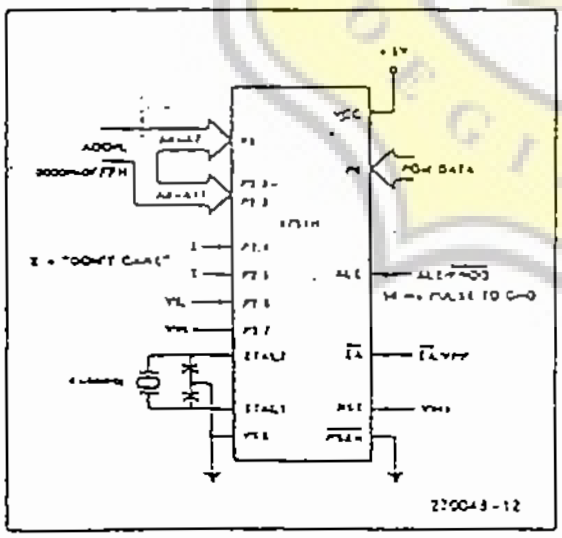


Figure 5. Programming Configuration

Note that the EA/VPP pin must not be allowed to go above the maximum specified VPP level of 21.5V for any amount of time. Even a narrow glitch above that voltage level can cause permanent damage to the device. The VPP source should be well regulated and free of glitches.

Program Verification

If the Security Bit has not been programmed, the on-chip Program Memory can be read out for verification purposes, if desired, either during or after the programming operation. The address of the Program Memory location to be read is applied to Port 1 and pins P2.0–P2.3. The other pins should be held at the "Verify" levels indicated in Table 3. The contents of the addressed location will come out on Port 0. External pullups are required on Port 0 for this operation.

The setup, which is shown in Figure 6, is the same as for programming the EPROM except that pin P2.7 is held at a logic low, or may be used as an active-low read strobe.

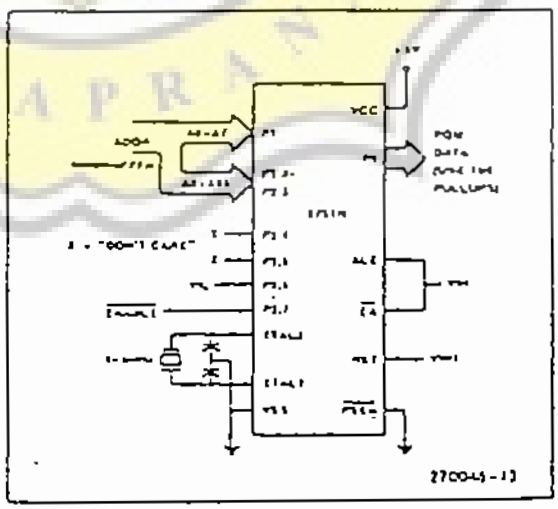


Figure 6. Program Verification

LAMPIRAN F

DATA BOOK IC 2764

EPROM Security

The security feature consists of a "locking" bit which when programmed denies electrical access by any external means to the on-chip Program Memory. The bit is programmed as shown in Figure 7. The setup and procedure are the same as for normal EPROM programming, except that P2.6 is held at a logic high, Port 0, Port 1, and pins P2.0–P2.3 may be in any state. The other pins should be held at the "Security" levels indicated in Table 3.

Once the Security Bit has been programmed, it can be cleared only by full erasure of the Program Memory. While it is programmed, the internal Program Memory can not be read out, the device can not be further programmed, and it can not execute out of external program memory. Erasing the EPROM, thus clearing the Security Bit, restores the device's full functionality. It can then be reprogrammed.

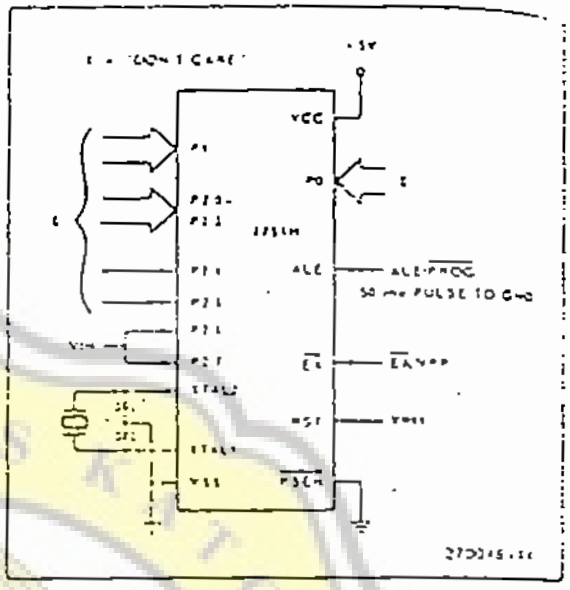


Figure 7. Programming the Security Bit

Erasure Characteristics

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 Angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Angstroms) to an integrated dose of at least 15 W-sec/cm². Exposing the EPROM to an ultraviolet lamp of 12,000 µW/cm² rating for 20 to 30 minutes, at a distance of about 1 inch, should be sufficient.

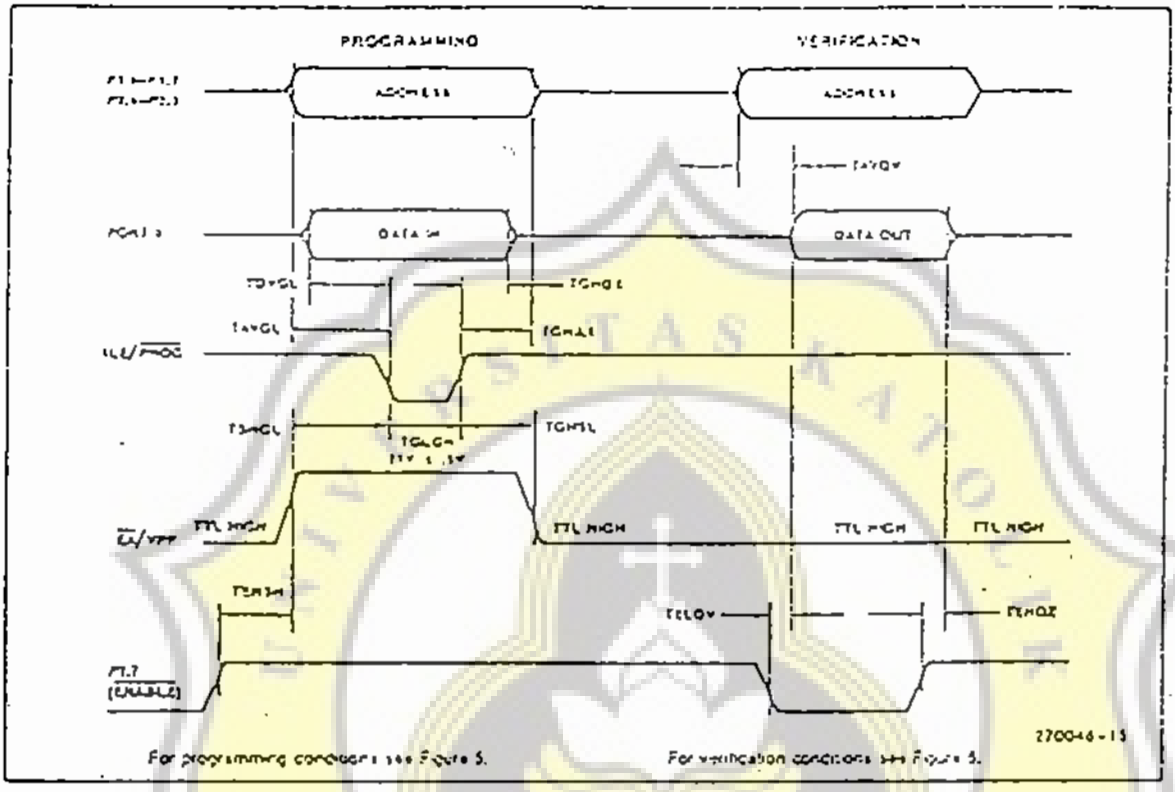
Erasure leaves the array in an all 1s state.

EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

T_A = 21°C to 27°C; VCC = 5V ±10%; VSS = 0V

Symbol	Parameter	Min	Max	Units
VPP	Programming Supply Voltage	20.5	21.5	V
IPP	Programming Supply Current		30	mA
1/TCLCL	Oscillator Frequency	4	6	MHz
TAVGL	Address Setup to PROG Low	48TCLCL		
TGHAX	Address Hold after PROG	48TCLCL		
TDVGL	Data Setup to PROG Low	48TCLCL		
TGHDX	Data Hold after PROG	48TCLCL		
TEHSH	P2.7 (ENABLE) High to VPP	48TCLCL		
TSHGL	VPP Setup to PROG Low	10		µs
TGHSL	VPP Hold after PROG	10		µs
TGLGH	PROG Width	45	55	ms
TAVQV	Address to Data Valid		48TCLCL	
TELQV	ENABLE Low to Data Valid		48TCLCL	
TEHQZ	Data Float after ENABLE	0	48TCLCL	

EPROM PROGRAMMING AND VERIFICATION WAVEFORMS



For programming conditions see Figure 5. For verification conditions see Figure 5.

DATA SHEET REVISION HISTORY

The following are the key differences between this and the -004 version of this data sheet.

1. Data sheet status changed from "Preliminary" to "Production".
2. LCC package offering deleted.
3. Maximum Ratings Warning and Data Sheet Revision History revised.

The following are the key differences between this and the -003 version of this data sheet:

1. Introduction was expanded to include product descriptions.
2. Package table was added.
3. Design Considerations added.
4. Test Conditions for I_{IL1} and I_{IH} specifications added to the DC Characteristics.
5. Data Sheet Revision History added.

74LS373, 74LS374, S373, S374
Latches/Flip-Flops

'373 Octal Transparent Latch With 3-State Outputs
'374 Octal D Flip-Flop With 3-State Outputs
Product Specification

Logic Products

FEATURES
- 8-bit transparent latch — '373
- 8-bit positive, edge-triggered register — '374
- 3-State output buffers
- Common 3-State Output Enable
- Independent register and 3-State buffer operation

DESCRIPTION
The '373 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Latch Enable (E) and Output Enable ($\overline{OE}$) control gates.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS373	19ns	24mA
74S373	10ns	105mA
74LS374	19ns	27mA
74S374	8ns	116mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N74LS373N, N74S373N, N74LS374N, N74S374N
Plastic SOL-20	N74LS373D, N74S373D, N74LS374D, N74S374D

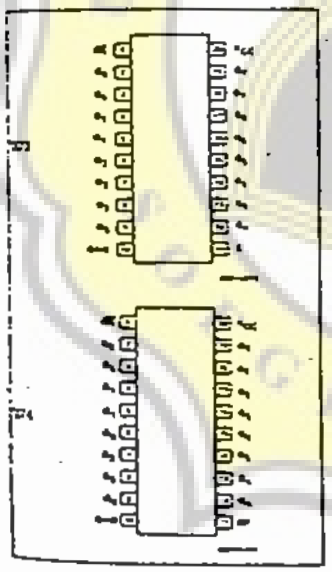
NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

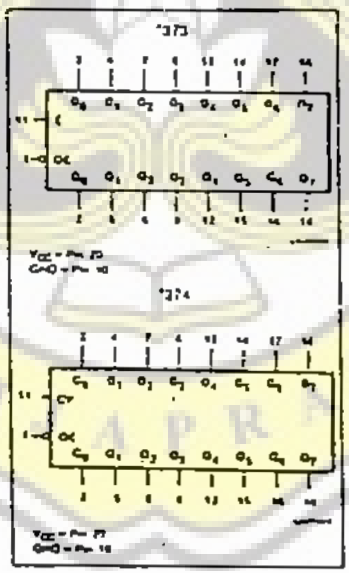
PINS	DESCRIPTION	74S	74LS
All	Inputs	1S.U	1LS.U
All	Outputs	10S.U	30LS.U

NOTE:
Where a 74S unit load (S.U) = 50μA I_{IL} and −2.0mA I_{OL}, and a 74LS unit load (LS.U) = 20μA I_{IL} and −0.4mA I_{OL}.

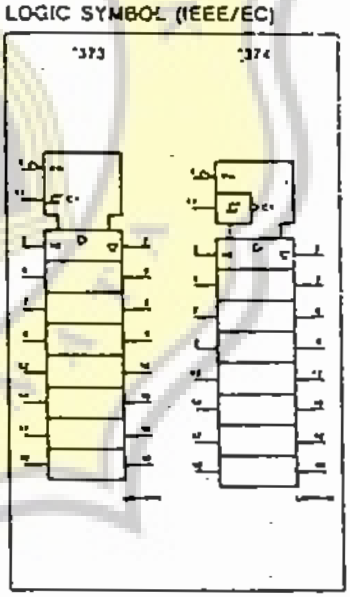
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/EC)



The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is HIGH. The latch remains transparent to the data inputs while E is HIGH, and stores the data present one set-up time before the HIGH-to-LOW enable transition. The enable gate has hysteresis built in to help minimize problems that signal and ground noise can cause on the latching operation.

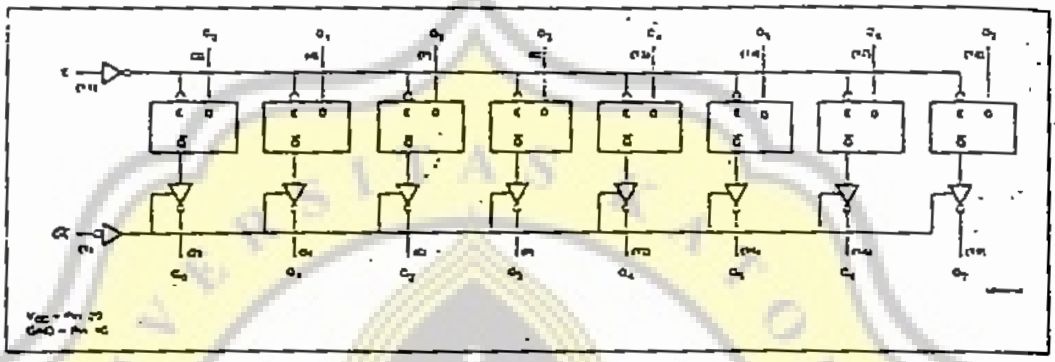
The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is LOW, the latched or transparent data appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

The '374 is an 8-bit, edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable ($\overline{OE}$) control gates.

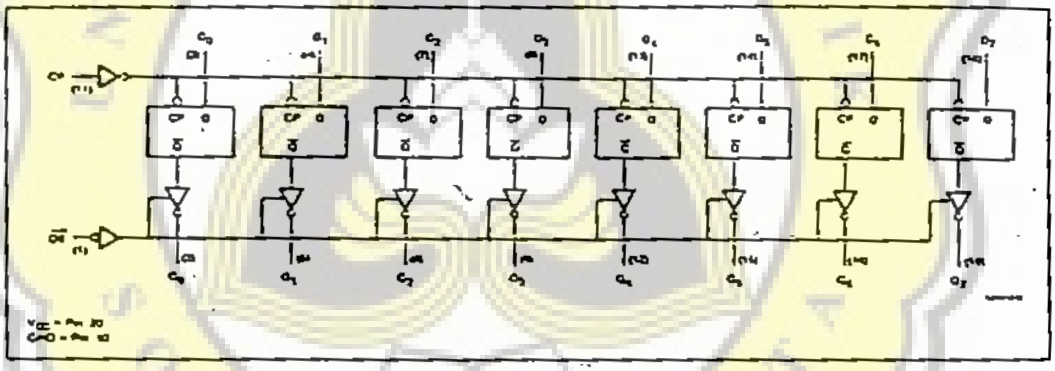
The register is fully edge triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The clock buffer has hysteresis built in to help minimize problems that signal and ground noise can cause on the clocking operation.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the register operation. When $\overline{OE}$ is LOW, the data in the register appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

LOGIC DIAGRAM, '373



LOGIC DIAGRAM, '374



MODE SELECT — FUNCTION TABLE '373

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	E	D_n		$O_0 - O_7$
Enable and read register	L	H	L	L	L
	L	H	H	H	H
Latch and read register	L	L	l	L	L
	L	L	h	H	H
Latch register and disable outputs	H	L	l	L	(Z)
	H	L	h	H	(Z)