# LAMPIRAN - LAMPIRAN

```
#include <STM32F4ADC.h>
#define H1 PB9
#define L1 PB8
#define H3 PB7
#define L3 PB6
#define H5 PD14
#define L5 PD13
#define H2 PD7
#define L2 PD6
#define H4 PD5
#define L4 PD4
#define H6 PD12
#define L6 PD11

STM32ADC inADC(ADC1);
int R_ref,S_ref,T_ref;
int R_act,S_act,T_act;
int R_err,S_err,T_err;
int SB = 1; //small band
int LB = 250; //large band
uint16_t analog_pins[] = {PA3, PA4, PA5, PA6, PA7, PC4, PC5};

void PINMODE() {
 pinMode(H1, OUTPUT);
 pinMode(H2, OUTPUT);
 pinMode(L1, OUTPUT);
 pinMode(L2, OUTPUT);
 pinMode(H3, OUTPUT);
 pinMode(H4, OUTPUT);
 pinMode(L3, OUTPUT);
 pinMode(L4, OUTPUT);
 pinMode(H5, OUTPUT);
 pinMode(H6, OUTPUT);
 pinMode(L5, OUTPUT);
 pinMode(L6, OUTPUT);
}
void setup() {
 Serial.begin(9600);
 PINMODE();
 for (uint16_t x = 0; x<sizeof(analog_pins); x++)
 pinMode(analog_pins[x], INPUT_ANALOG);
```

```
 Timer2.init();
 Timer2.pause();
 Timer2.setMasterMode(TIMER_MASTER_MODE_UPDATE);
 Timer2.setPeriod(15);
 Timer2.setMode(TIMER_CH2, TIMER_OUTPUT_COMPARE);
 Timer2.setCompare(TIMER_CH2, 1);
 Timer2.attachInterrupt(TIMER_CH2,INT1);
 Timer2.refresh();

 Timer3.init();
 Timer3.pause(); // stop timer
 Timer3.setMasterMode(TIMER_MASTER_MODE_UPDATE);
 Timer3.setPeriod(15);
 Timer3.setMode(TIMER_CH3, TIMER_OUTPUT_COMPARE);
 Timer3.setCompare(TIMER_CH3, 3);
 Timer3.attachInterrupt(TIMER_CH3,INT2);
 Timer3.refresh();
 Timer2.resume();
 Timer3.resume();

 inADC.setSamplingTime(ADC_SMPR_3);
 inADC.enableDMA();
}

void loop() {
 //Serial.println(R_ref);
 }
void INT1(void){
 R_ref = map(analogRead(PC4),0,4095,-2000,2000);//referensi
 R_act = map(analogRead(PA6),0,4095,-4000,4000);//actual
 R_err = R_ref - R_act;

 S_ref = map(analogRead(PC5),0,4095,-1700,1700);//referensi
 S_act = map(analogRead(PA5),0,4095,-4000,4000);//actual
 S_err = S_ref - S_act;

 T_ref = map(analogRead(PA3),0,4095,-2000,2000);//referensi
 T_act = map(analogRead(PA4),0,4095,-4000,4000);//actual
 T_err = T_ref - T_act;
}
void INT2(void){ //jkff
 R();
 S();
 T();
 }
void R(){
```

```
 if (R_err > SB){
  digitalWrite(H1,1);
  digitalWrite(L1,0);
 }
 if (R_err < -SB){
  digitalWrite(H1,0);
  digitalWrite(L1,1);
 }

 if (R_err > LB){
  digitalWrite(H2,0);
  digitalWrite(L2,1);
 }
 if (R_err < -LB){
  digitalWrite(H2,1);
  digitalWrite(L2,0);
 }
}
void S(){
// digitalWrite(H3,0);
// digitalWrite(H4,0);
// digitalWrite(L3,0);
// digitalWrite(L4,0);
 if (S_err > SB){
  digitalWrite(H3,1);
  digitalWrite(L3,0);
 }
 if (S_err < -SB){
  digitalWrite(H3,0);
  digitalWrite(L3,1);
 }
```

# A Simple Hysteresis Control Strategy in Voltage Regulated Three Phase Four Wire System for Photovoltaic Application

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**Abstract-** Photovoltaic energy is expected to be the future sustainable source of clean energy. However, photovoltaic energy could only produce DC output that must be converted to AC for three-phase four-wire (3P4W) system implementation. Therefore, a highly efficient DC-AC inverter is required to utilize this photovoltaic energy fully. This study proposes and implements a new simple control strategy into the 3P4W inverter to produce a high-quality output voltage. This topology has three one-phase full-bridge topology inverters connected in parallel and operated in a high-switching frequency system to achieve a suitable output voltage waveform. Therefore, the proposed strategy must support high switching frequency performance and maximize it into a maximum achievable switching capability, namely double band hysteresis with a frequency limiter. The proposed strategy aims to adjust the switching frequency for all components of the 3P4W inverter to achieve its maximum capabilities. Hence, the quality of output voltage generated has high efficiency and sustainably. The resulted output voltage confirmed the combination of the proposed topology and control strategy works well by producing a smooth sinusoidal AC waveform. The performance of the 3P4W inverter is evaluated by using Total Harmonic Distortion (THD) Calculation which has a value of 2.68%. Referring to the resulted THD value proves the proposed control strategy operates efficiently and effectively. This study presents a new control strategy to contribute to the modern application of power conversion which focuses on control techniques by using green energy sources and systems in the form of implementing photovoltaic applications.

**Keywords** Photovoltaic energy; Three-phase four-wire system; Voltage regulated inverter; Frequency limiter; Double band hysteresis.

## 1. Introduction

The development of energy conversion systems increases in line with developments in the energy technology sector. Nowadays, the energy technology sector highly values reliable and affordable energy sources [1]. This notion popularizes the widespread use of photovoltaic applications in distributed power generation systems [2, 3]. Photovoltaic application for electricity distribution system typically uses a three-phase four-wire (3P4W) system, which requires an inverter [4, 5, 6]. A 3P4W inverter converts DC energy from Photovoltaic to an AC energy system. The Photovoltaic is used as the green energy source for the 3P4W inverter. The inverter development focused on implementing a new topology and control strategy to improve conversion efficiency. The less value of Total Harmonic Distortion generated, the better its development of it. The topology commonly used in 3P4W inverter are three-phase four-leg topology [7], and 3P4W split DC bus topology [8], which produces a high-stress level of voltage. The high-stress level of voltage causes the components to become hot and a shortage of voltage inside the components and circuits. To prevent and fix those problems, this study proposes a 3P4W topology composed of three one-phase full-bridge inverter topologies connected in parallel to prevent a high-stress level of voltage. This topology needs a high switching frequency to gain a good waveform result [9].

This study proposes a simple strategy to control the proposed 3P4W inverter topology. The purpose of the proposed new simple strategy control is to adjust the output voltage to keep track of a given reference value and minimize energy losses. One of the simple strategies, hysteresis, is usually used because of its superiority in terms of stability, quick performance, and easy implementation [10, 11]. A simple single-band hysteresis is typically used to control and inherently limit the voltage [12, 13]. This control strategy has a single band hysteresis which has an upper and lower band. This control strategy produces a stable Pulse

Width Modulation signal. Hence, the output voltage generated has good quality. Still, the switching frequency is unnecessarily high because the zero-level output voltage is not produced [14, 15]. A high level of switching frequency can cause an increase in energy loss in the power switch's semiconductor. The zero-output voltage must be applied to prevent it. To utilize the zero-output voltage, a double-band hysteresis control strategy is used [16]. This strategy uses two bands; each controls a pair of power switches [17]. The small hysteresis band serves to form the output voltage, and the large band serves to change its polarity [18]. The conventional double band hysteresis control strategy produces a unipolar Pulse Width Modulation signal which has zero level output voltage. The weaknesses of the proposed strategy are uncontrollable switching frequency [19]. It creates an unbalanced switching frequency of the components in the system consisting of a microcontroller, drivers, and power switches. As a result, this issue leads to inefficient power consumption. The inefficient power consumption is led by the produced Pulse Width Modulation signal with a high switching frequency which instructs the power switches to be switched into the next logic value before its time for it to transfer the energy completely. This event occurs when the switching frequency exceeds the limit of the maximum switching frequency of the components. As stated before, the proposed design topology needs a high switching frequency to gain good results for the waveform but if the switching frequency exceeds the limit of the components, the produced energy losses are high and the waveform is not in good condition. As a result, the switching frequency must be modified to fully exploit the switching devices' capabilities [20, 21, 22].

This study focuses on the proposed control strategy in the 3P4W and the photovoltaic control where a maximum power point tracking (MPPT) had not been exposed. For the MPPT, its system control and algorithm are used to maximize and determine the output generated by photovoltaics [23, 24]. The system control and algorithm of MPPT are not explained and discussed in this paper. Furthermore, the proposed control uses a simple new hysteresis strategy, double-band hysteresis with a frequency limiter. This study contributes to improving the performance of the 3P4W inverter by implementing the proposed new control strategy by combining it with the proposed topology design to be able to accurately track the given reference value, and directly create a new control strategy for the energy conversion system which is an upgraded version of the existing control strategy. The proposed strategy limits the switching frequency of all components below the specified value and adjusts it to a maximum achievable value [25, 26]. The logical gated flip flop is used to limit the frequency value [27, 28]. The logical flip flop is been used to get the fundamental function of it where the value of the clock determines the logical value generated [29]. The value of the clock is used as the frequency limit. If the switching frequency exceeds the frequency of the clock, the switching cannot be passed to power switches [30]. This proposed control strategy uses a conventional double band hysteresis control strategy as the base for it and is upgraded in combination with a frequency limiter. The double band hysteresis has two bands to shape the output voltage and change the polarity of the output voltage. Each band works as a limiter for the actual value to keep track of the reference value. The value of the output voltage must not change when the load is changed. The double band hysteresis has a role for maintains the waveform of the actual signal to prevent the waveform from being distorted. The frequency limiter has a crucial part in this new control strategy. This study discusses the resulting impact on the output voltage by implementing the proposed strategy in the 3P4W inverter topology in terms of effectiveness and efficiency. This statement is proven by the value of Total Harmonic Distortion (THD) generated by the output voltage [31]. This study also covers the interaction between the proposed control strategy and design topology in the 3P4W system for Photovoltaic Application as green energy sources.

## 2. Inverter Operation and Control Strategy

### *2.1. Circuit Design Configuration*

The proposed design of the three-phase four-wire inverter is shown in Fig. 1. The inverter topology is formed from three one phase full-bridge inverters connected in parallel. Each one phase full bridge inverter produces a one-phase AC wave which has different phase angles of 120 degrees from one another. The first phase is at a phase angle of 0 degrees, the second phase is at a phase angle of 120 degrees, and the third phase is at a phase angle of 240 degrees. The output side of each inverter is connected to the primary side of the transformer. The phase and neutral points are connected in a star connection on the secondary side of the transformer. Thus, a three-phase four-wire system is obtained.

### *2.2. Switching Operation Modes*

A one-phase full-bridge inverter topology is the most basic variant of the proposed 3P4W inverter design. To improve efficiency, four conditions are used to generate positive, negative, and zero level output voltages (shown in Figs. 2–5) [32].

As shown in Fig. 2, Condition one is obtained when MSFT1 and MSFT4 power switches are ON. Thus, positive fluctuation is generated. Figure 2 shows that the DC power $V_{DC}$ passes the current through MSFT1 and MSFT4 power switches and the inductive filter to loads. Condition one can be calculated as Eq. (1) to (4).

$$V_{DC} = V_{(out)} + V_{(L)} \tag{1}$$

$$V_{DC} - V_{(out)} = L\frac{di_{(L)}}{dt} \tag{2}$$

$$\Delta T \,.\, (V_{DC} - V_{(out)}) = L\Delta i_{(L)} \tag{3}$$

$$T_{(on)} \,.\, (V_{DC} - V_{(out)}) = L\Delta i_{(L)} \tag{4}$$

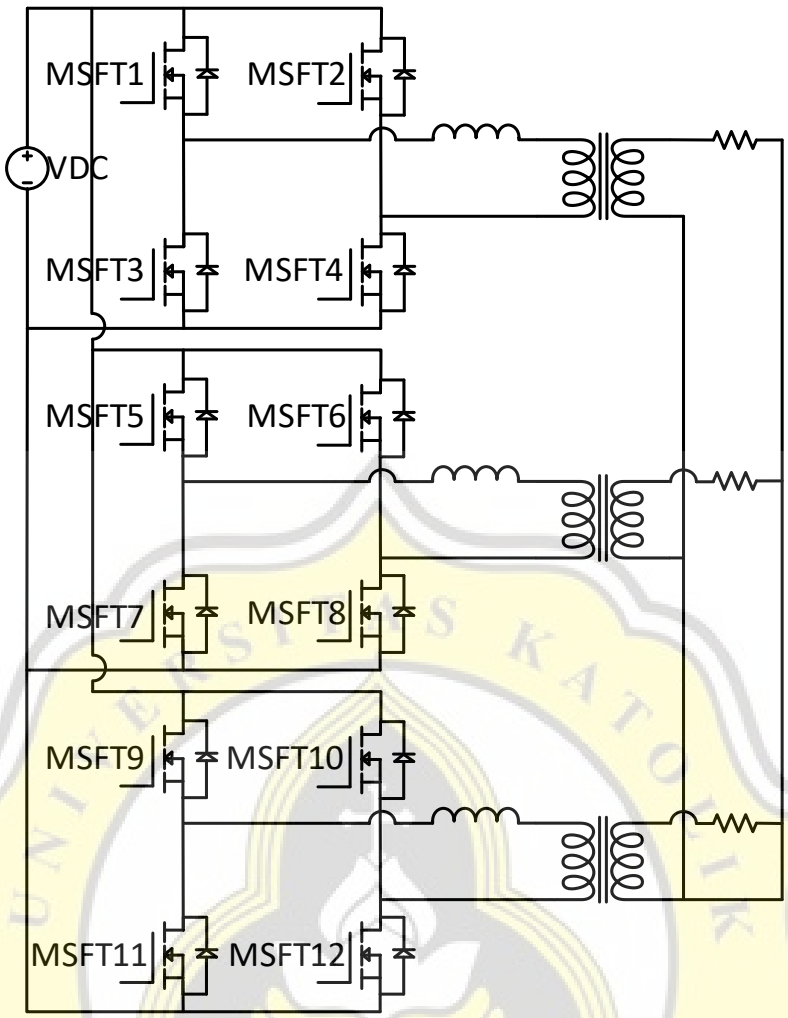



**Fig. 1.** Circuit Design of Three Phase Four Wire Inverter Topology.

Condition two is obtained in Fig. 3 when MSFT1 and MSFT2 power switches are ON. The freewheeling condition is achieved in this condition. This condition generates the zero-level output voltage. The inductive current flows to loads and flows through MSFT2 and MSFT1 power switches back to load. Condition two is expressed as Eq. (5) to (8).

$$V_{(out)} + V_{(L)} = 0 \tag{5}$$

$$V_{(out)} - 0 = L\frac{di_{(L)}}{dt} \tag{6}$$

$$\Delta T \,.\, (V_{(out)}) = L\Delta i_{(L)} \tag{7}$$

$$T_{(off)} \,.\, (V_{DC} - V_{(out)}) = L\Delta i_{(L)} \tag{8}$$

When MSFT2 and MSFT3 power switches are ON, condition three is achieved, as seen in Fig. 4. The DC power E passes current through MSFT2 and MSFT3 power switches to loads. This condition generates negative fluctuations, as Eq. (9) to (12).

$$-V_{DC} = V_{(out)} + V_{(L)} \tag{9}$$

$$-V_{DC} - V_{(out)} = L\frac{di_{(L)}}{dt} \tag{10}$$

$$\Delta T \,.\, (-V_{DC} - V_{(out)}) = L\Delta i_{(L)} \tag{11}$$

$$T_{(on)} \,.\, (-V_{DC} - V_{(out)}) = L\Delta i_{(L)} \tag{12}$$

As seen in Fig. 5, The current flows from inductive filter to loads through MSFT3 and MSFT4 power switches. Figure 5 shows that the MSFT3 and MSFT4 power switches are ON; therefore, condition four is obtained. Hence, the freewheeling condition is achieved. In this condition, it generates zero-level output voltage. Condition four can be calculated as Eq. (13) to (16).

$$0 = V_{(out)} + V_{(L)} \tag{13}$$

$$V_{(out)} - 0 = L\frac{di_{(L)}}{dt} \tag{14}$$

$$\Delta T \,.\, (V_{(out)}) = L\Delta i_{(L)} \tag{15}$$

$$T_{(off)} \,.\, (V_{(out)}) = L\Delta i_{(L)} \tag{16}$$

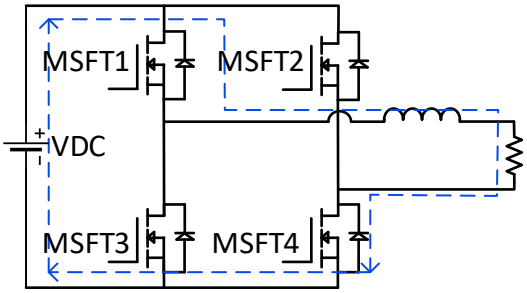



**Fig. 2.** Condition One.

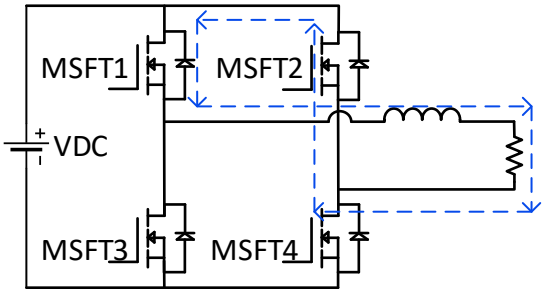



**Fig. 3.** Condition Two.

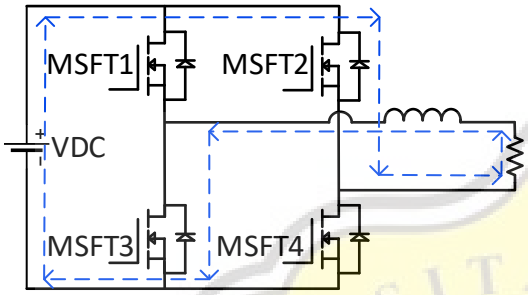



**Fig.4.** Condition Three.

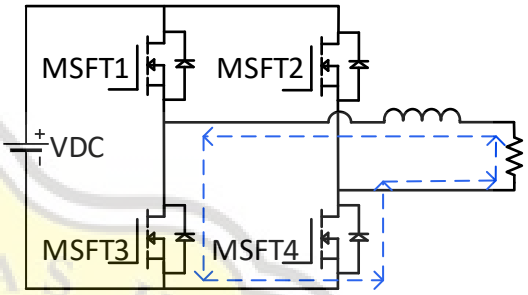



**Fig. 5.** Condition Four.

*2.3. Switching Control Strategy*

The conditions 1 to 4 are constructed by the Pulse Width Modulation (PWM) switching pattern, as seen in Table 1. The logical value in Table 1 must be achieved to obtained the desired value of the output voltage. The proposed control strategy is used as a voltage controller and has the fundamental way of working as the conventional double band hysteresis to use a unipolar PWM technique, referred to in Table 1. The unipolar PWM technique produce a PWM signal which work as switching pattern and the speed of the PWM signal produced is described as the switching frequency.

**Table 1.** PWM Logical Switches

| Logical Value | | | | Vout |
|---|---|---|---|---|
| MSFT1 | MSFT2 | MSFT3 | MSFT4 | |
| 1 | 0 | 0 | 1 | $+V_{DC}$ |
| 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | $-V_{DC}$ |
| 0 | 0 | 1 | 1 | 0 |

Figure 6 shows the double band hysteresis control strategy. It has two bands, small and large hysteresis bands. The small hysteresis band is operated as a barrier band. Depending on the error, it generates two switching states, ON and OFF. The small hysteresis band has the preset upper and lower hysteresis band as the limiter for error value. The small hysteresis band controls MSFT3 and MSFT4 power switches.

If the error value exceeds the preset upper hysteresis band ($H_{s+}$), the power switches are operated off. During this state $T_{OFF}$, the output voltage is zero where *h* changes to – *h* and it can be described in equations as in Eq. (17). the power switches are operated in ON state if the error is exceeds the preset lower hysteresis band ($H_{s-}$), then, denoted by $T_{ON}$, which can be calculated as Eq. (18).

$$T_{OFF} = \frac{L\Delta i_{(L)}}{V_{(out)}} \tag{17}$$

$$T_{ON} = \frac{L\Delta i_{(L)}}{(V_{DC} - V_{(out)})} \tag{18}$$

In positive or negative cycle, the current flowing overtime interval $T_{(off)}$ is the result of the difference of the current from the initial condition and the current $\Delta i$. This condition is expressed as Eq. (19) to (23). Thus, the output voltage and current value are expressed as Eq. (23) and Eq. (24). The connection between the output voltage and current is described as Eq. (25).

$$(V_{DC} - V_{(out)}) \cdot T_{(on)} = V_{(out)} \cdot T_{(off)} \tag{19}$$

$$V_{DC} \cdot T_{(on)} - V_{(out)} \cdot T_{(on)} = V_{(out)} \cdot T_{(off)} \tag{20}$$

$$V_{DC} \cdot T_{(on)} = V_{(out)} \cdot (T_{(on)} + T_{(off)}) \tag{21}$$

$$V_{DC} \cdot T_{(on)} = V_{(out)} \cdot T_s \tag{22}$$

$$V_{(out)} = V_{DC} \cdot \frac{T_{(on)}}{T_s} = D \cdot V_{DC} \tag{23}$$

$$I_{(out)} = I_m \cdot \sin\theta \tag{24}$$

$$\frac{I_m \cdot Z}{V_{DC}} = \frac{V_{(out)}}{V_{DC}} \tag{25}$$

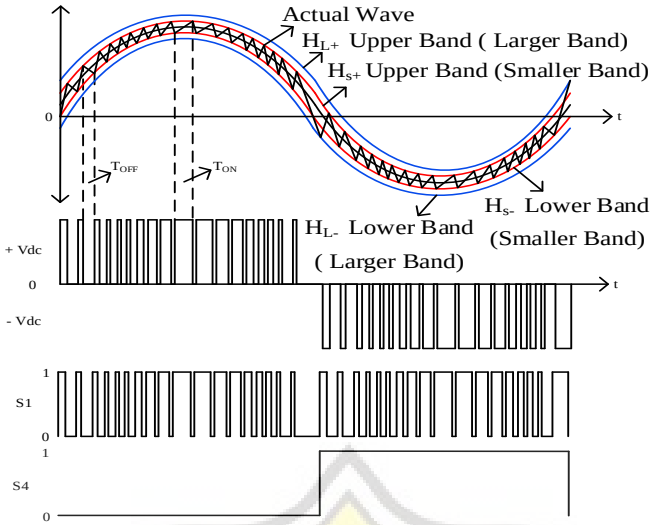



**Fig. 6.** Switching Sequences of Double band hysteresis control strategy.

The small hysteresis band controls and determines the majority of the output voltage error. When the small hysteresis band is unable to handle an error, the large hysteresis band reacts. The small hysteresis band forms the output voltage, whereas the large hysteresis band alters the polarity of the output voltage. Unipolar PWM Switching is present in the output voltage. In real-time, the switching frequency generated by this strategy cannot be adjusted, and it can exceed the limits of the capabilities possessed by each component. It creates a switching frequency imbalance in the system, which cause inefficiency in power consumption. Therefore, the switching frequency should be limited to an achievable frequency of each component to create a balanced system.

Figure 7 shows the creation of the two cycles of the inverter. The wave above the zero-level voltage creates the positive output voltage by producing the pulse width modulation signal. The frequency limiter is implemented in one of the power switches to limit the frequency produced. When the wave is below the zero-level voltage, the negative output voltage is generated. It worked on the same principle: a frequency limiter limits the frequency of one or both of the power switches. The switching period must be obtained by using the equations as Eq. (26). Thus, the switching frequency produced is expressed as Eq. (27) and Eq. (28).

$$T_s = T_{(on)} + T_{(off)} = \frac{V_{DC} L \Delta i_{(L)}}{V_{(out)}(V_{DC} - V_{(out)})} \quad (26)$$

$$f_s = \frac{L\Delta i_{(L)}}{8V_{(o)}C} = \frac{(V_{DC} - V_{(out)})D}{L\Delta i_{(L)}} \quad (27)$$

Based on Eq. (28), the switching frequency produced must be matched in the calculation as Eq. (30). The sensitivity of the switching frequency produced is measured by changing the function into its derivative form as Eq. (29), and it must be equal to zero as Eq. (30) to gain a maximum switching frequency.

$$f_s = \frac{D \sin\theta(1 - D \sin\theta)}{4Li_{(L)}} \quad (28)$$

$$\frac{df_s}{d\theta} = \frac{(D - 2D^2 \sin\theta)\cos\theta)}{4L\Delta i_{(L)}} \quad (29)$$

$$\frac{df_s}{d\theta} = 0 \quad (30)$$

Based on Eq. (30), the maximum angle must be matched as Eq. (31), and the value of D requires a value as Eq. (32) to achieve a zero value. By using Eq. (31) and Eq. (32) into Eq. (28), the switching frequency can be expressed as Eq. (33). The value of switching frequency is determined by using the modulation system. If the modulation system of control strategy only uses one sinusoidal waveform, the switching frequency produced can be calculated by using Eq. (33). If the modulation system of control strategy uses two sinusoidal waveforms in which the other sinusoidal waveform is inverted, it causes the switching frequency to have a value twice the value of Eq. (33), and it can be calculated as Eq. (34).

$$\sin\theta = \frac{1}{2D} \quad (31)$$

$$D = \frac{1}{2} \quad (32)$$

$$f_s = \frac{1}{4L\Delta i_{(L)}} \quad (33)$$

$$f_{maximum} = \frac{1}{2 \,.\, 4L\Delta i_{(L)}} = \frac{1}{8L\Delta i_{(L)}} \quad (34)$$

By applying the logical gated flip flop, it is possible to determine the switching frequency of Pulse Width

Modulation generated. The frequency limiter is shown in Fig. 9. The preset frequency limit is determined by changing the clock frequency value. The PWM is passed if the clock frequency value is above the value of switching frequency and vice versa. Figure 10 describes the scheme of the proposed strategy control, namely the double band hysteresis control strategy with frequency limiter. The input of the control strategy consists of the actual output and the reference. The scheme of the proposed control strategy is applied to a programming flowchart, as seen in Fig. 8. The interrupt function enables to limit the frequency produced. Interrupt one is used by the double band hysteresis control strategy to generate the PWM, and interrupt two is used to arrange frequency limiter value. The conventional double band hysteresis is modified into the proposed control strategy as a frequency limiter and still maintains the quick response characteristic of the hysteresis controller.

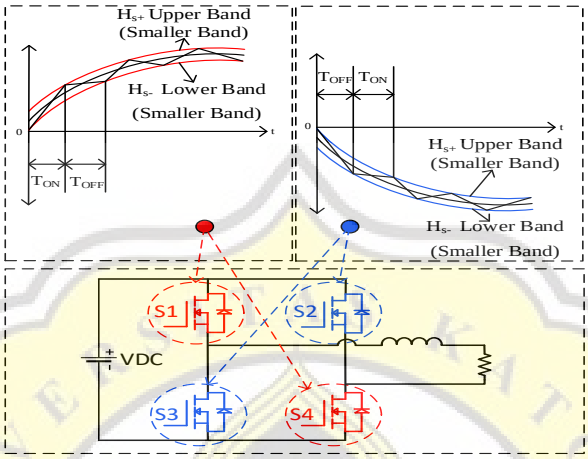



**Fig. 7.** Double band hysteresis voltage controller.

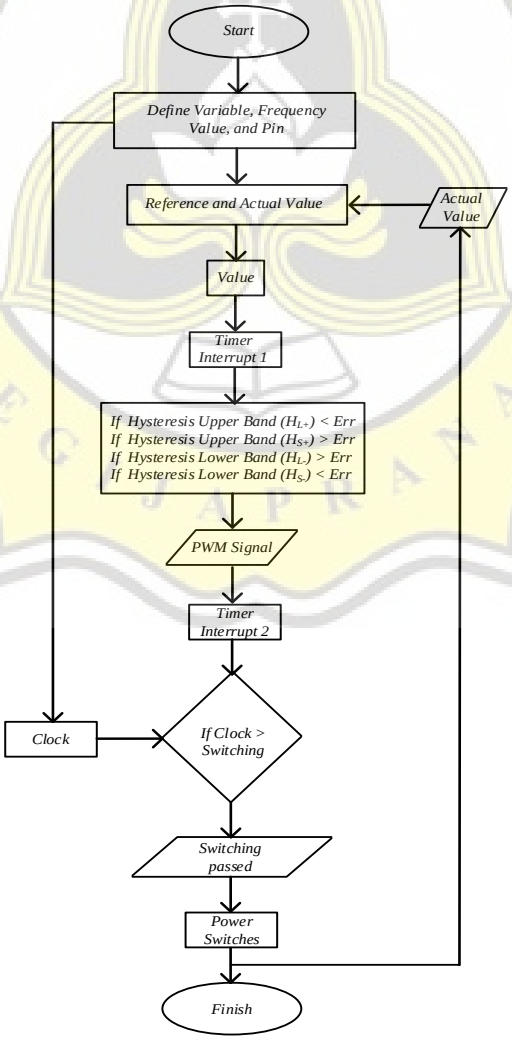



**Fig. 8.** Programming Flowchart.

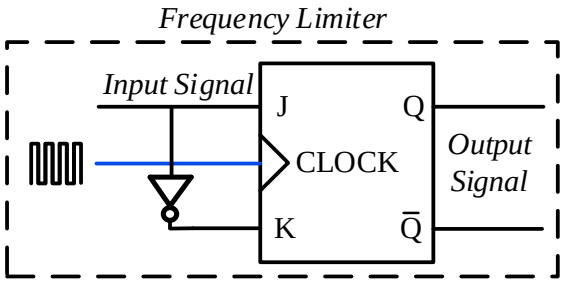



**Fig. 9.** Frequency Limiter.

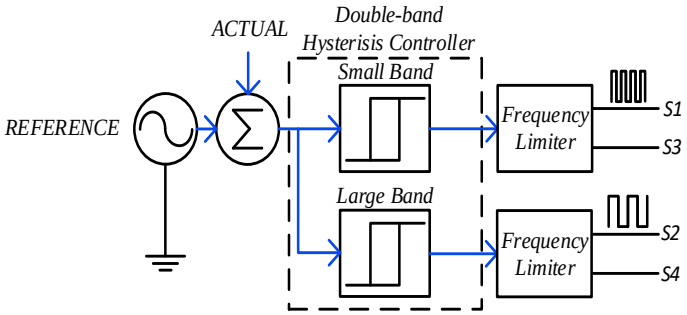



**Fig. 10.** Control strategy scheme.

## 3. Results and Analysis

The proposed control strategy is proven by using computational simulation and implemented in hardware to verify its validity. The proposed topology design is simulated in Real-time simulation using PSIM software by Power SimTech. The parameter value for Real-time simulation and hardware implementation is shown in Table 2. The hardware is shown in Fig. 11. The hardware implementation is captured and shown using an oscilloscope to display the outut of 3P4W inverter. Based on Fig.12 and Fig.13, the PWM signals show no difference between the pulse width modulation generated by simulation or hardware implementation. The output voltage before and after filtering is shown in Figure 14. Fig. 15 illustrates the output voltage and current. The output voltage has a THD value of 2,68 percent shown in Fig.19, according to the IEEE standard [33]. The THD value is measured by consider the fundamental components which is 50 Hz, and the harmonic components. The output voltage and current responses when the load value is changed are shown in Figure 16. Based on Fig. 16, the proposed control strategy successfully controls the output voltage and still maintains a stable value of the waveform, it does not shrink or rise when the value of the load changes in the middle of time. The change of load value is shown by the changing value of the output current. Based on Fig. 17 and Fig. 18 show the output voltage and current generated by a 3P4W inverter. Figures 12 – 18 cover the Real-time simulation and hardware implementation result which captured in Real-time play. The proposed strategy results maintain a quick response from the conventional hysteresis strategy, and the switching frequency is kept within certain limits. Therefore, the output voltage produces a low THD value and has high efficiency. High efficiency in the conversion system generated less energy losses. The output voltage tracks accurately against a given reference signal. Hence, when a load is changed the output voltage retains its shape.

**Table 2.** Simulation and Hardware Parameters

| ***Device*** | ***Units*** |
|---|---|
| Voltage DC | 30 Volt |
| DC Power Supply | 12 – 15 Volt |
| Inductor | 2 mH |
| Value of Load 1 | 1200 Watt |
| Value of Load 2 | 600 Watt |
| Hysteresis Upper Band (Smaller Band) | 0.01 V |
| Hysteresis Lower Band (Smaller Band) | – 0.01 V |
| Hysteresis Upper Band (Larger Band) | 0.2 V |
| Hysteresis Lower Band (Larger Band) | – 0.2 V |
| Transformer Step Up | 1: 6.29 |
| Clock Frequency | 25 kHz |
| Frequency of Interrupt Function 1 | 25 kHz |
| Frequency of Interrupt Function 2 | 25 kHz |
| Reference waveform Amplitude | 2.8 V |
| Reference waveform Frequency | 50 Hz |

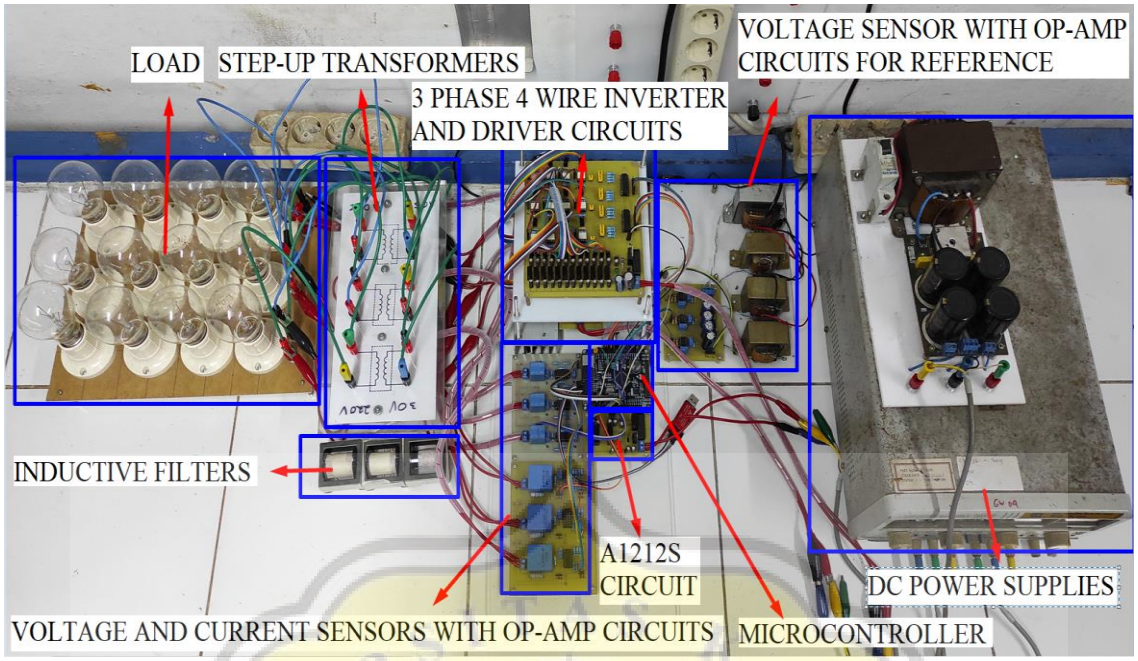
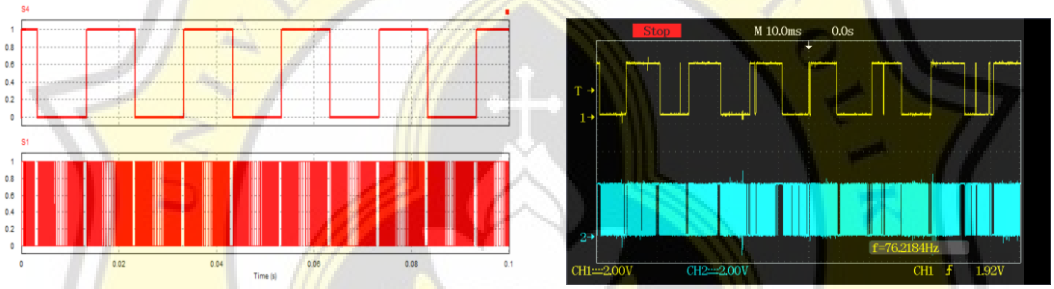
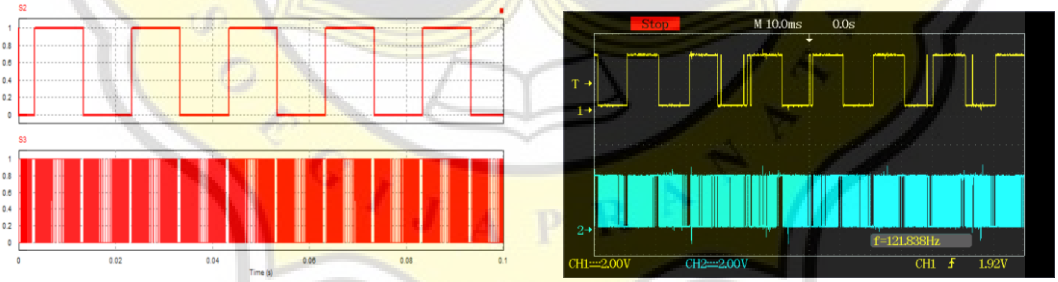



**Fig. 11.** Three phase four wire Inverter hardware.



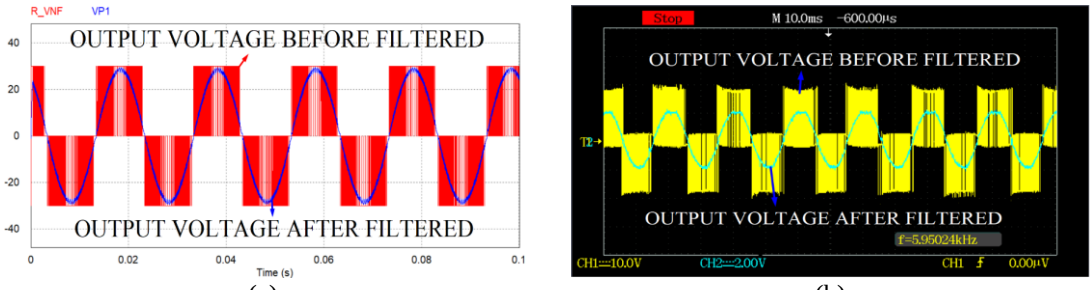

(a) (b)

**Fig. 12.** PWM for MSFT1 and MSFT4: (a) simulation, (b) hardware.



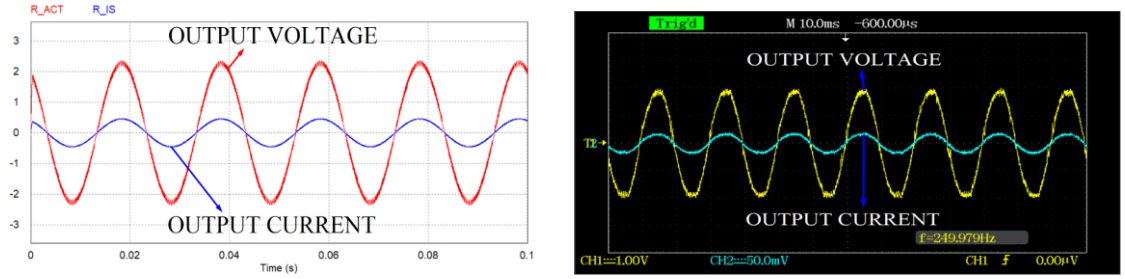

(a) (b)

**Fig. 13**. PWM for MSFT2 and MSFT3: (a) simulation, (b) hardware.



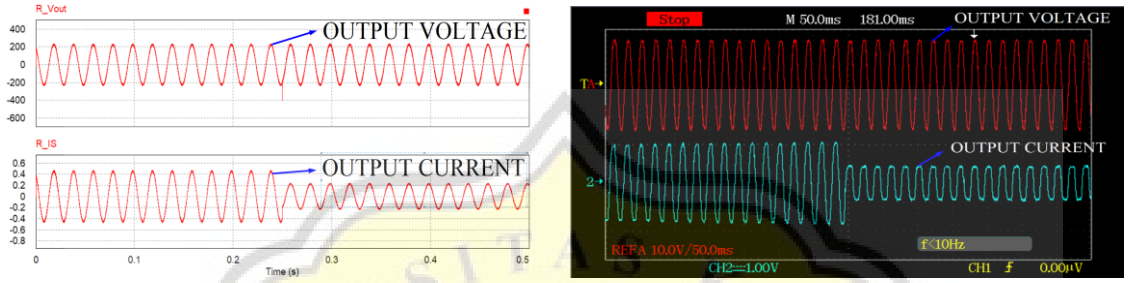

(a) (b)

**Fig.14**. Output voltage before and after filtered: (a) simulation, (b) hardware.



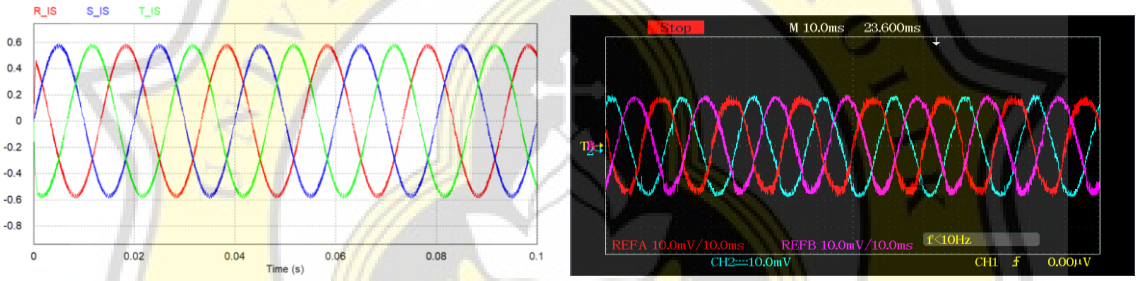

(a) (b)

**Fig. 15**. Output voltage and current: (a) simulation, (b) hardware.



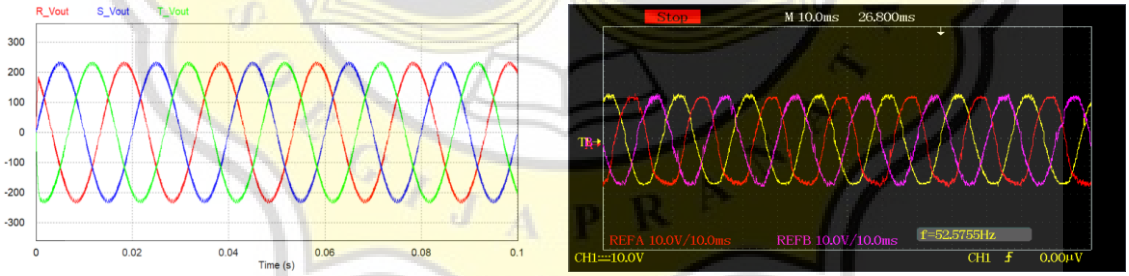

(a) (b)

**Fig.16.** The response of load value variations: (a) simulation, (b) hardware.




(a) (b)

**Fig.17.** Three phase four wire output current: (a) simulation, (b) hardware.




(a) (b)

**Fig. 18**. Three phase four wire output voltage: (a) simulation, (b) hardware.

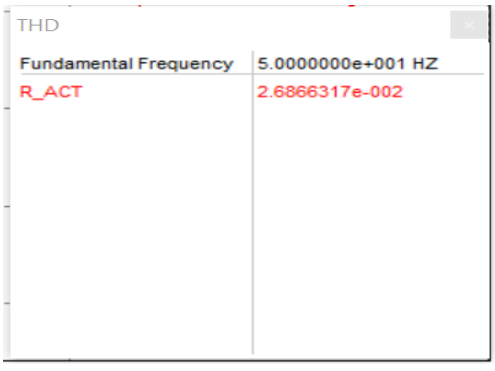



**Fig.19.** THD value based on Real-Time Simulation.

## 4. Conclusion

This study mainly covers the proposed control strategy and design for the 3P4W inverter. It presents a simple hysteresis voltage controller. The proposed control strategy uses the conventional double band hysteresis strategy with a frequency limiter to limit the generated switching frequency. Hence, the system works quickly and generates a unipolar PWM (better waveform). The switching frequency is adjusted and limited to the maximum achievable value of the components. By limiting the switching frequency of each element to a given value, the proposed control approach can establish a balanced system. Thus, the 3P4W inverter's capabilities are completely utilized, and energy dissipation on the power switch's semiconductor is minimized.

The proposed design configuration is modified for Photovoltaic application. A photovoltaic system is used as a DC power generator. The DC power generated by Photovoltaic cells is maximized using a maximum power point tracker. The 3P4W inverter uses DC power to generate 3P4W AC output. Implementing the proposed control strategy into the proposed design of the 3P4W inverter has successfully created a perfect combination which is proved by the 2.68% of THD value. The resulting THD value is below the IEEE 519 standards (5 %). Based on laboratory research, the output voltage successfully maintains its value when the load value is changed.

Based on this study, it can be concluded that the proposed control strategy, namely the double band hysteresis strategy with a frequency limiter has succeeded in producing a good quality 3P4W AC voltage as evidenced by its THD value and remains constant. This study contributes in the form of the development of control techniques to improve efficiency in the energy conversion system which uses a green energy system as a source for the 3P4W distribution system where energy losses are minimized during the conversion process. The focus for further work is to improve the system's efficiency and get less THD value which can be done by modifying the proposed control strategy or implementing it in the advanced topology of a 3P4W inverter.

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