LAMPIRAN

1. **Program Inverter 3 Fasa 4 Kawat *double-loop control***

```
#include <STM32F4ADC.h>
#define H1 PB9
#define L1 PB8
#define H3 PB7
#define L3 PB6
#define H5 PD14
#define L5 PD13
#define H2 PD7
#define L2 PD6
#define H4 PD5
#define L4 PD4
#define H6 PD12
#define L6 PD11

STM32ADC inADC(ADC1);
int count,car,conr,cons,cont;
int R_ref,S_ref,T_ref;
int R_actv,S_actv,T_actv;
int R_acti,S_acti,T_acti;
int err,I,lastI,pi,f;
float kp=1;
float ki=1;
int SB = 1;  //small band
uint16_t analog_pins[] = {PA0, PA1, PA2, PA3, PA4, PA5, PA6, PA7, PC4,
PC5};

void PINMODE() {
 pinMode(H1, OUTPUT);
 pinMode(H2, OUTPUT);
 pinMode(L1, OUTPUT);
 pinMode(L2, OUTPUT);
 pinMode(H3, OUTPUT);
 pinMode(H4, OUTPUT);
 pinMode(L3, OUTPUT);
```

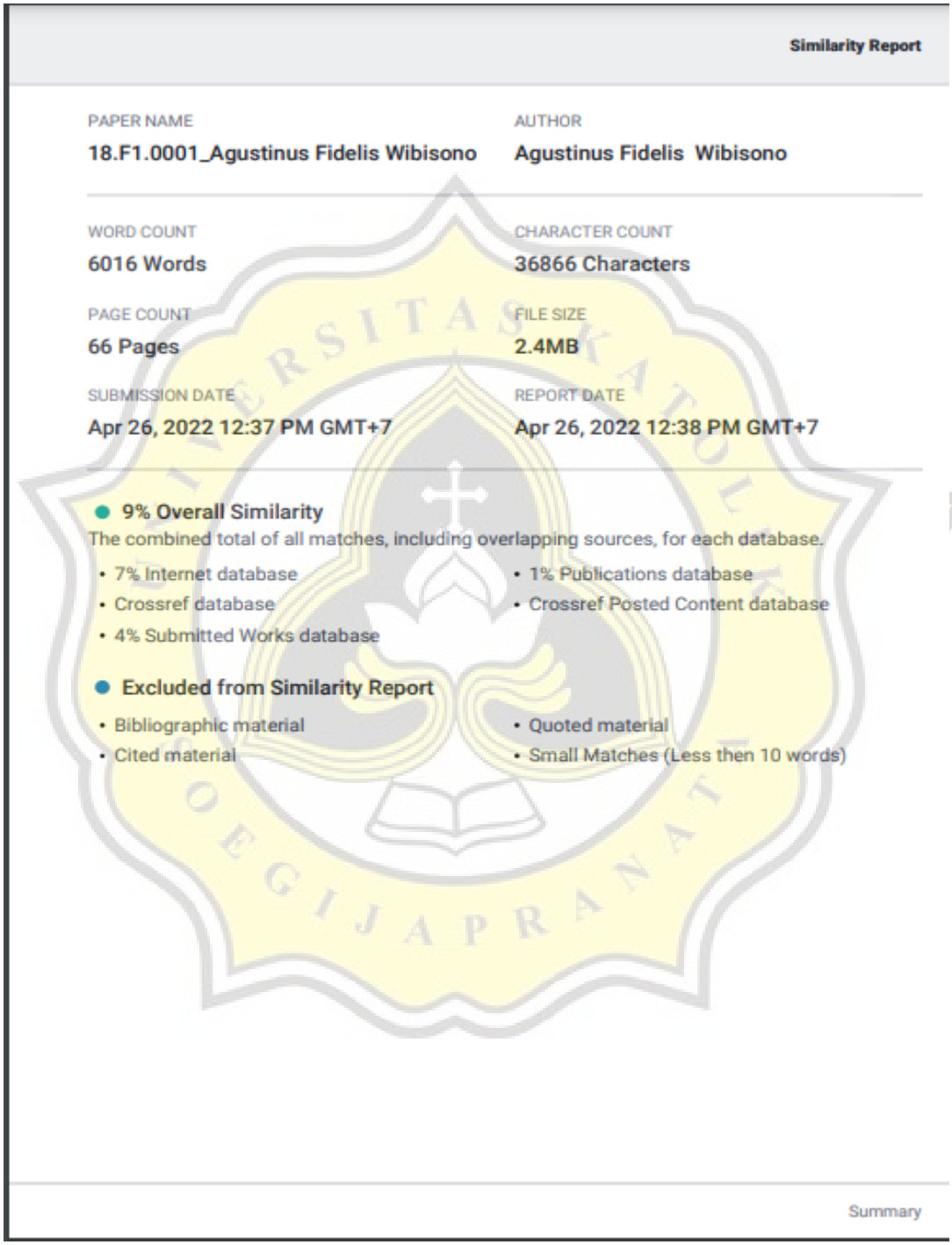
```
 pinMode(L4, OUTPUT);
 pinMode(H5, OUTPUT);
 pinMode(H6, OUTPUT);
 pinMode(L5, OUTPUT);
 pinMode(L6, OUTPUT);
}
void setup() {
 //Serial.begin(9600);
 PINMODE();
 for (uint16_t x = 0; x<sizeof(analog_pins); x++)
 pinMode(analog_pins[x], INPUT_ANALOG);

 Timer2.init();
 Timer2.pause();
 Timer2.setMasterMode(TIMER_MASTER_MODE_UPDATE);
 Timer2.setPeriod(20);
 Timer2.setMode(TIMER_CH2, TIMER_OUTPUT_COMPARE);
 Timer2.setCompare(TIMER_CH2, 1);
 Timer2.attachInterrupt(TIMER_CH2,INT1);
 Timer2.refresh();
 Timer2.resume();

 inADC.setSamplingTime(ADC_SMPR_3);
 inADC.enableDMA();
}

void loop() {
 R();
 S();
 T();
}

int kontrol(int ref, int act, int acti){
 err = ref - act;
 I = ki*err*lastI*0.00001;
 lastI = I;
 pi = (kp*err) + I;
```

```
 f = pi - acti;
}

void INT1(void){
 R_ref = map(analogRead(PC4),0,4095,-4000,4000);//referensi
 R_actv = map(analogRead(PA6),0,4095,-4000,4000);//actual
 R_acti = map(analogRead(PA2),0,4095,-4000,4000);
 conr = kontrol(R_ref,R_actv,R_acti);

 S_ref = map(analogRead(PC5),0,4095,-2000,2000);//referensi
 S_actv = map(analogRead(PA5),0,4095,-4000,4000);//actual
 S_acti = map(analogRead(PA1),0,4095,-4000,4000);
 cons = kontrol(S_ref,S_actv,S_acti);

 T_ref = map(analogRead(PA3),0,4095,-2000,2000);//referensi
 T_actv = map(analogRead(PA4),0,4095,-4000,4000);//actual
 T_acti = map(analogRead(PA0),0,4095,-4000,4000);
 cont = kontrol(T_ref,T_actv,T_acti);
}

void R(){
  if (R_ref > 0){
    digitalWrite(H2,0);
    digitalWrite(L2,1);
    digitalWrite(L1,0);
    if(conr > SB)
      digitalWrite(H1,1);
    if(conr < -SB)
      digitalWrite(H1,0);
  }
  if (R_ref < 0){
    digitalWrite(H2,1);
    digitalWrite(L2,0);
    digitalWrite(H1,0);
    if(conr > SB)
      digitalWrite(L1,0);
    if(conr < -SB)
```

```
    digitalWrite(L1,1);
  }
}
void S(){
  digitalWrite(H3,0);
  digitalWrite(H4,0);
  digitalWrite(L3,0);
  digitalWrite(L4,0);

  if (S_ref > 0){
    digitalWrite(H4,0);
    digitalWrite(L4,1);
    digitalWrite(L3,0);
    if(cons > SB)
     digitalWrite(H3,1);
    if(cons < -SB)
     digitalWrite(H3,0);
  }
  if (S_ref < 0){
    digitalWrite(H4,1);
    digitalWrite(L4,0);
    digitalWrite(H3,0);
    if(cons > SB)
     digitalWrite(L3,0);
    if(cons < -SB)
     digitalWrite(L3,1);
  }
}
void T(){
  digitalWrite(H5,0);
  digitalWrite(H6,0);
  digitalWrite(L5,0);
  digitalWrite(L6,0);
  if (T_ref > 0){
    digitalWrite(H6,0);
    digitalWrite(L6,1);
    digitalWrite(L5,0);
```

```
  if(cont > SB)
    digitalWrite(H5,1);
  if(cont < -SB)
    digitalWrite(H5,0);
}
if (T_ref < 0){
  digitalWrite(H6,1);
  digitalWrite(L6,0);
  digitalWrite(H5,0);
  if(cont > SB)
    digitalWrite(L5,0);
  if(cont < -SB)
    digitalWrite(L5,1);
}
```

Plagiarsm Check



Similarity Report

PAPER NAME
18.F1.0001_Agustinus Fidelis Wibisono

AUTHOR
Agustinus Fidelis Wibisono

WORD COUNT
6016 Words

CHARACTER COUNT
36866 Characters

PAGE COUNT
66 Pages

FILE SIZE
2.4MB

SUBMISSION DATE
Apr 26, 2022 12:37 PM GMT+7

REPORT DATE
Apr 26, 2022 12:38 PM GMT+7

9% Overall Similarity
The combined total of all matches, including overlapping sources, for each database.

- 7% Internet database
- Crossref database
- 4% Submitted Works database
- 1% Publications database
- Crossref Posted Content database

Excluded from Similarity Report

- Bibliographic material
- Cited material
- Quoted material
- Small Matches (Less then 10 words)

Summary

Design and Implementation of Double Loop Control Strategy in TPFW Voltage and Current Regulated Inverter for Photovoltaic Application

Leonardus Heru Pratomo [1], Agustinus Fidelis Wibisono [2], Slamet Riyadi [3]
[1, 2,3] Department of Electrical Engineering, Soegijapranata Catholic University, Semarang, Indonesia
Email: [1] leonardus@unika.ac.id, [2] fidelis.wibi@gmail.com, [3] riyadi@unika.ac.id

***Abstract*—Increasing demands for renewable energy encourage the development of inverters as a solution for converting energy from direct photovoltaic current (DC) output to alternative current (AC) at a maximum output power. Several nation standard systems are three-phase four-wired (TPFW), which means that the TPFW inverter must be used. The issue arises because the TPFW inverter is operated through an open-loop system, which has the problem of preventing the inverter from adjusting the voltage and current as needed. Hence, the open-loop system must be converted to a closed-loop system which is usually used only single control. The single strategy control is not effective because this strategy cannot regulate voltage and current at the same time. It only controls either voltage or current. The output voltage or current is changed when the load value is changed. Due to its weaknesses, the study proposes a new double-control strategy method that utilizes a PI strategy (P) controller as a voltage controller and a proportional strategy control as a current controller. This strategy is tested and measured by using simulation, showing a THD value of 1.07%. Accordance to IEEE standards, the THD value is within the recommended limit. Therefore, the output voltage and current produced have a good signal with a low ripple and stability without fluctuation.**

Keywords—Inverter; Photovoltaic; PI; proportional; THD; voltage control; current control; MPPT

I. INTRODUCTION

Increasing development in power electronics becomes critical in a modern environment, and it is the core of the latest application energy conversion system [1]-[4]. Flexibility in utilization creates a technical hurdle in terms of the control method and topology used [5]. These TPFW inverters are commonly used for the application of hybrid power systems based on renewable energy [6]-[8]. These converter advancements are primarily used in renewable energy and industrial appliances. The method works by processing the output of the photovoltaic in the direct current (DC) form. After that, MPPT will maximize the direct current (DC) output power, and the last, direct current output power will be converted to alternate current (AC) by inverter as a source for industrial and home appliances [9]-[12].

The 3-phase inverter topology usually uses three pairs of power switches that have losses at high voltage and require high frequencies and a large inductor [13]-[15]. TPFW inverters generally utilize a three-phase four-leg configuration, which results in a high-stress level of voltage [20][26][30]. To archive the minimum of stress in the generated voltage, this study proposes a new TPFW configuration. In this study, the TPFW inverter was created according to the presented topology. The inverter itself has two types of control, which are voltage and current controlled inverter [16]. The output voltage is produced on a three-phase four-wire commonly regulated by an open-loop system. However, the major disadvantage of the open-loop system is the voltage and current cannot be adjusted as desired [17][25][29]. As a result, a control strategy is utilized by the TPFW inverter to modulate the output voltage and current [19]. Even the solution cannot solve all the problems, such as it produces an unstable sinusoidal waveform when passing through zero level output voltage [18][21]. The actual output voltage cannot follow the reference signal quickly because of fluctuation, and the resulting current is distorted. The impact of these problems is inefficiencies in power consumption. To solve this problem, the open-loop system must be converted to a closed-loop system, usually only a single control strategy. When a non-linear load is used in an industrial application, the voltage and current are usually distorted. As a result, the control strategy must be responsible for controlling both the output voltage and current. This strategy of double-loop control is required.

In order to resolve those problems, the needs for a new control strategy that can control the output voltage and current at the same time are crucial. This paper proposes a new method of control strategy called double-loop strategy control three-phase four-wired voltage and current regulated inverter. This method is the combination of switching using control strategy PI (proportional integrator), which is used as a voltage controller, and a proportional control strategy used as a current controller. The double-loop control demonstrated in this study produced a steady signal and reduced distortion caused by the non-linear load. When the value of the load is changed, the output voltage and current are not distorted. This strategy has been confirmed through computational simulation and hardware implementation utilizing the STM32F407 microcontroller. This research focuses on inverter and system control but also demonstrates how this strategy improves the output voltage and current regulated.

II. INVERTER OPERATION AND CONTROL STRATEGY

This work employs a procedure that includes a theoretical background, statement of the problem, simulation, implementation detail, and testing to arrive at a conclusion. A theoretical review of the TPFW inverter was conducted, and several issues were uncovered, leading to the formulation of the inverter difficulty. Using power simulator (PSIM)

software, a simulation was run to ensure that the hardware design would function. The conclusion is reached after the creation and testing of hardware.

A. Inverter Three-Phase Four-Wired and Strategy Control

Fig. 1 shows the topology inverter three-phase four-wired (TPFW). Inverter three-phase four wired is a combination of three full-bridge inverters connected to each other using a single DC source.

The transformer used for inverter three-phase four-wired has two winding, namely primary winding N_p and the secondary winding N_s. The number-based comparison number between the secondary winding and primary winding can determine the primary voltage V_d and secondary voltage V_i on the transformer. To determine the value of the winding and transformer voltage (T_F), shown by the equation (1).

$$T_F = \frac{V_d}{V_i} = \frac{N_s}{N_p} \quad (1)$$

According to Fig. 1, each of the inverters has a 120° shift angle for output current. The transformer is used to interconnect each phase of the inverter from the primary side (T1, T2, T3) to the output using the wye technique. The angle of the first phase from the transformer secondary side (T1) is 0° degrees for the second phase from the transformer secondary side (T2) is 120° degrees, and the of the third phase (T3) is 240 degrees [23]-[27].

B. Inverter Switching Mode Operation

The latest research on double-loop control for the TPFW system was the result of modifying a full-bridge inverter consisting of four power switches semiconductors that operate on high power applications. The four power switches of the full-bridge inverter can be controlled by two operation modes, namely bipolar and unipolar. The topology full-bridge inverter is illustrated in Fig. 2.

As depicted in Fig. 2, in this mode of operation, the power switch semiconductor PSS1 and PSS4 conduct, and the current load comes from the DC link (+E) across PSS1, then through the resistor as the load, and back to the source through the resistor bypassing the power switch PSS4. As a result of this process, the output voltage is positive [21][28]. The equation of operation mode 1 is described in (2) to (5).

$$E = V_{(L)} + V_{(o)} \quad (2)$$

$$L\frac{di_{(L)}}{dt} = E - V_{(o)} \quad (3)$$

$$L\Delta i_{(L)} = \Delta t.(V_{(o)} - E) \quad (4)$$

$$L\Delta i_{(L)} =. t_{(on)}.(V_{(o)} - E) \quad (5)$$

The second mode of operation is a freewheeling mode. There are two stages in this condition positive cycle and negative cycle. The polarity from voltage through load changes to inductive load, and PSS3 and PSS4 are disabled in this mode to prevent the inverter from floating. Freewheeling occurs as a result of the L filter collecting electric current in the form of the magnetic field PSS1 and PSS2 ON to generate a zero-level output voltage. The operation mode 3, the current flows from the power switch PSS2 to the inductor to the R load, then passes through the PSS2 power switch semiconductor diode and back to the inductor as the filter. The equation of operation mode 2 and 3 is described in (6) to (9).

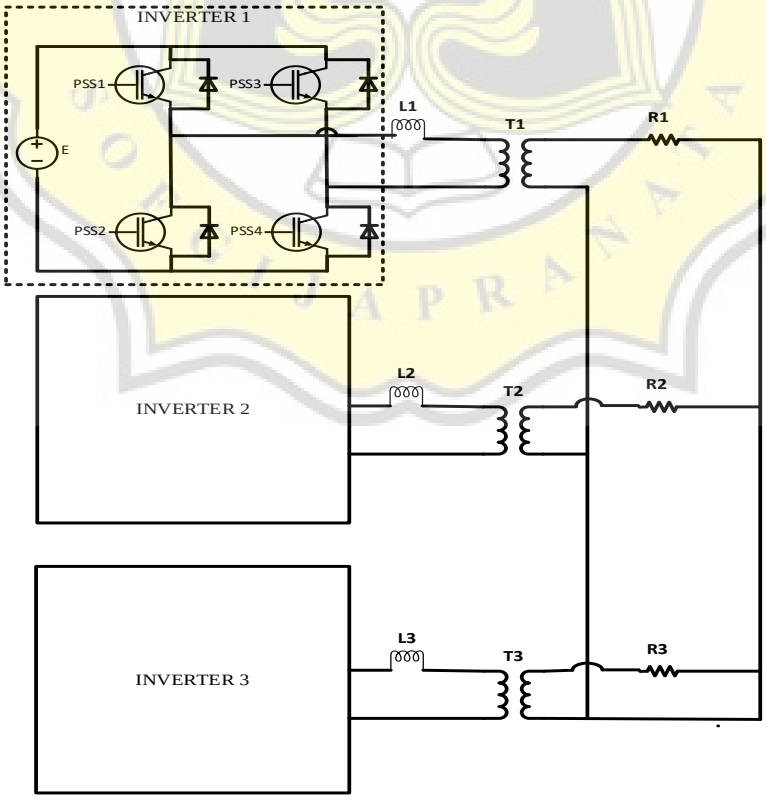


Fig. 1. Topology TPFW inverter

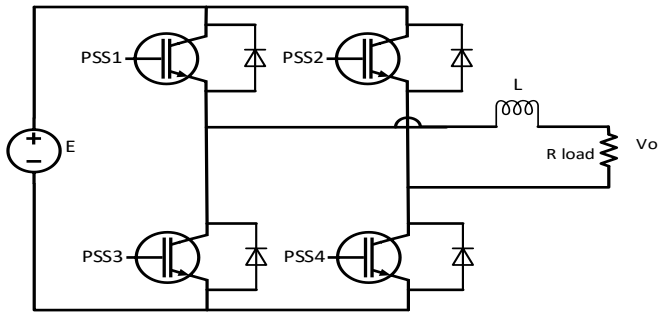


Fig 2. Topology full-bridge inverter

$$V_L = V_{(0)} + V_{(d)} \quad (6)$$

$$L\frac{di_{(L)}}{dt} = V_{(0)} - 0 \quad (7)$$

$$\Delta t.\left(V_{(o)}\right) = L\Delta i_{(L)} \quad (8)$$

$$t_{(off)}.\left(V_{(o)}\right) = L\Delta i_{(L)} \quad (9)$$

Operation mode 4, PSS2, and PSS4 will be conducted. From that, the current flow from the DC source (E) will pass PSS2 through the load and back to the DC source, passing the PSS4, and producing a negative output voltage [29]-[30]. Operation mode 4 is expressed in equations (10) and (12).

$$-E = V_{(o)} + V_{(L)} \quad (10)$$

$$-E - V_{(o)} = L\frac{di_{(L)}}{dt} \quad (11)$$

$$V_{(o)} = m\,E \quad (12)$$

The transfer function of inverter and transformer (Kinv) is as follows

$$Kinv_F = m\frac{N_s}{N_p} \quad (13)$$

Where m = modulation index

C. Strategy Control

The control circuit is required to enable the power circuit to operate a semiconductor power switch. The strategy control is composed of two components the power circuit and the control circuit. The power is composed of (PSS1-PSS4), and also the SPWM is calculated utilizing the proposed strategy control. Both the reference and real power grid signals are determined using the voltage sensor. The reference signal and the actual voltage are compared, and the difference is calculated using a proportional-integral controller. The calculated value will be decremented by the current rate. For final result will be processed by a proportional controller to achieve switching PSS1 and PSS2, while PSS3 and PSS4 generate zero-crossing detection to enable the inverter to operate in unipolar mode. Fig. 7 illustrates the power and control schematic.

This flowchart in Fig. 8 depicts the program when the current and voltage sensor read the actual signal, and the state electrical company creates a signal of reference. Subtract that reference signal voltage from the signal voltage to obtain an error value. Using the PI control equation, the error signal will be processed, and the estimated result is decremented to correspond actual current signal. The value will be evaluated against the error using P control in order to generate PWM from the logic gate during power switching. The STM32F407 microcontroller implements this double-loop control TPFW inverter control circuit. The microcontroller is used to read the reference and sensor signal.

A proportional controller (P) is the simplest system for implementing a continuous control strategy in a closed-loop system. The proportional control strategy minimizes process variable fluctuation. It also gives a faster reaction than the majority of other control methods, initially allowing the proportional control strategy to respond a few seconds faster. However, as the strategy control becomes more complicated, the difference in response time may compound, allowing the proportional control to reply several minutes faster [14][16]. Proportional control generates a deviation from the set-point referred to as an offset. Proportional (P) control establishes a linear correlation between controller output (actual signal) and the error. The control function proportional controller has shown in equation (14).

$$P = K_p \quad (14)$$

Thus, the proportional (P) control method establishes a linear link between the error value system and the output control system. Proportional (P) control gives a reaction depending on the signal regulating the system. Otherwise, any oscillation is eradicated, and the system will return to a steady state, the set-point, the signal, and bias. The proportional (P) strategy control calculates the difference between the set-point and the signal, which is the error value these values will be transmitted to and the algorithm. Bias will be paired with the error value this algorithm indicated that the controller should take.

Adjusting the voltage is accomplished by the use of a proportional-integral controller (PI), a closed-loop control method that is a combination of proportional and integral control. By comparing the present and previous values of an error value, the proportional plus integral controller may restore the real signal to the reference point. The control function proportional plus integral controller is in equation (15).

$$p_I = K_P + \frac{1}{T_{is}} \quad (15)$$

Where P_I as the controller output K_p was proportional gain T_{is} as integrator gain.

D. Double Loop Control

The voltage-current control system is a type of double closed-loop control. This comparison is made between the output voltage and the reference waveform, and the divergence is sent off to the outer PI controller, where it serves as the reference for the output current. The current control system is obtained after comparing the result of the outer PI controller with the actual output current, and then it will be calculated by the inner P controller. The system

control block diagram is shown in Fig. 3. The comparison process for the value of P to process the PWM output signal from the inverter K_{INV} then the output signal is processed by filtering (L+R) to produce a smooth sinusoidal waveform.

Fig. 4 illustrates the system model block diagram of a double-loop control scheme in which the voltage is controlled by PI, (G_{CV}) to create a stable voltage loop. Fig. 5 illustrates the voltage control system to process the PI algorithm. The equation demonstrates in (16) to (17).

$$\frac{V_O}{V_{ref}}=\frac{SK_p+K_i}{S^3tC+S^2C+S.K_P+K_i} \quad (16)$$

$$\frac{V_O}{V_D}=\frac{S^2t+S}{S^3tC+S^2C+SK_p+K_i} \quad (17)$$

The value compared to the current P control ($G_{CI)}$ to produce the current regulated value, based on Fig. 6 shows the regulated current control system from the system shows the equation (18) to (19).

$$\frac{I_O}{I_{ref}}=\frac{G_{CI}.K_{INV}}{L+G_{CI}.K_{INV}} \quad (18)$$

$$\frac{I_o}{I_{ref}}=\frac{K_{INV}.K_P}{L+K_p.K_{INV}} \quad (19)$$

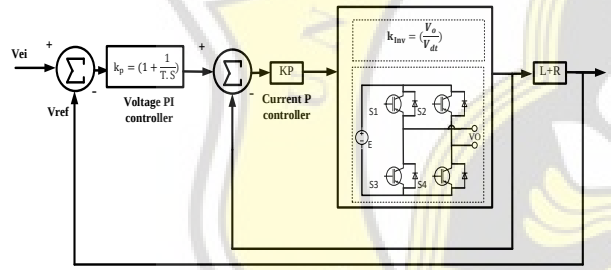


Fig. 3. Double-loop control system

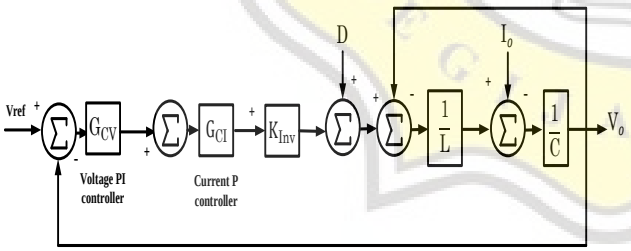


Fig. 4. System model block diagram

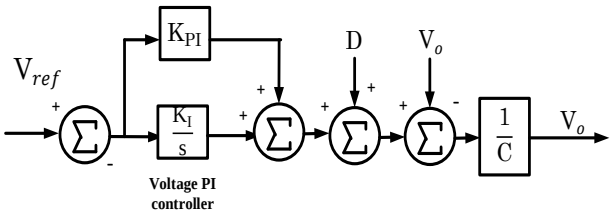


Fig. 5. Voltage control system

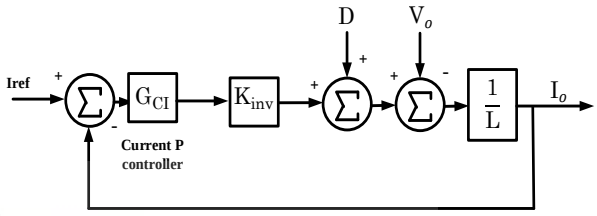


Fig. 6. Current control system

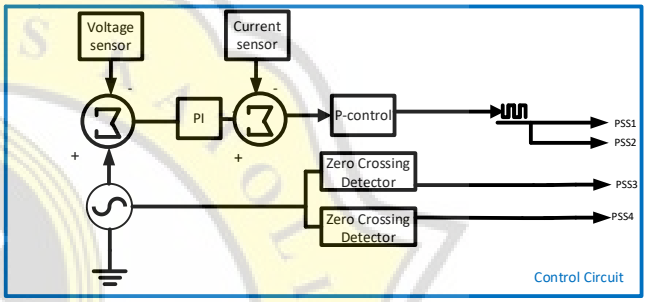


Fig. 7, Power circuit along with inverter three-phase four-wired control circuit

From the current calculation value of P, the value compared with an inverter to produce a waveform, the signal output needs a filter to produce sinusoidal voltage output for the inverter. The equation is described in (20).

$$K_{INV}=(\frac{V_o}{V_{d_t}}) \quad (20)$$

III. RESULT AND ANALYSIS

The TPFW inverter double-loop control was designed using power simulation (PSIM) software and developed in the laboratory. The simulation and hardware implementation parameters are shown in Table 1.

From Fig. 9, the hardware implementation uses an R, S, T phase for the reference from the state electricity company, LEM HX-10P as a current sensor, and LV-25P as the voltage sensor, TLP 250 as a driver, and STM32F407 as a microcontroller, inductor as the L filter, lamp as the non-linear-load, the IGBT used running to a high and low frequency of power switching.

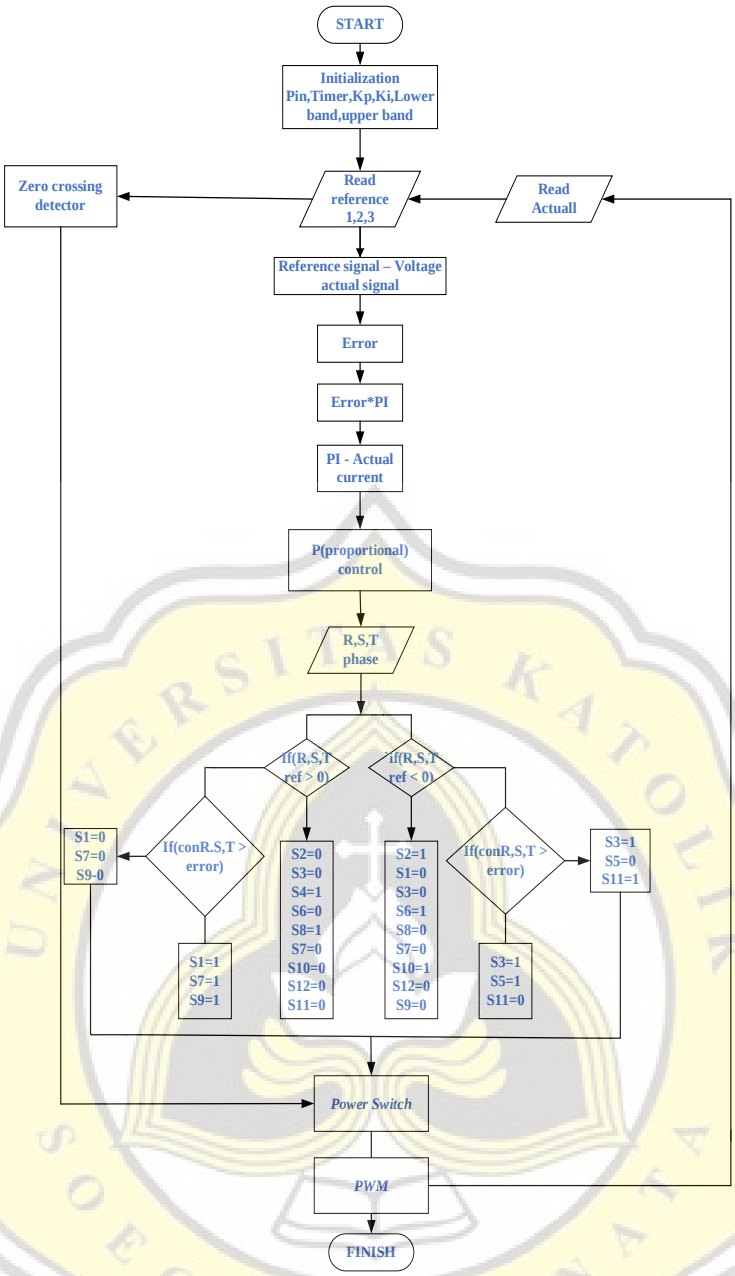


Fig. 8. Flowchart program

TABLE I. TABLE TYPE STYLES

NO	*PARAMETER*	*VALUE*
1	DC Power supply	32V
2	Inductor	1mH
3	Load	1200watt
4	Step-up Transformer	1 : 6.29
5	Switching frequency	5Khz
6	Kp Value	1
7	Ki value	1

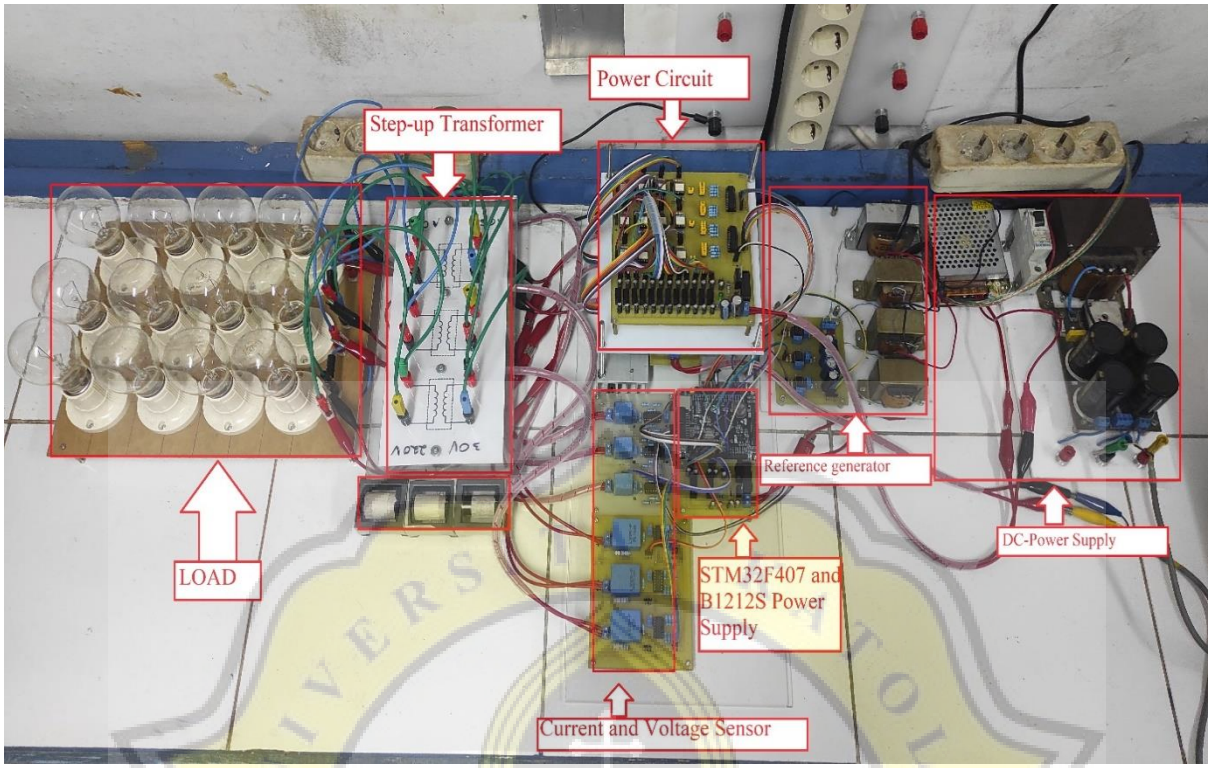


Fig 9. Hardware implementation double loop TPFW-Inverter

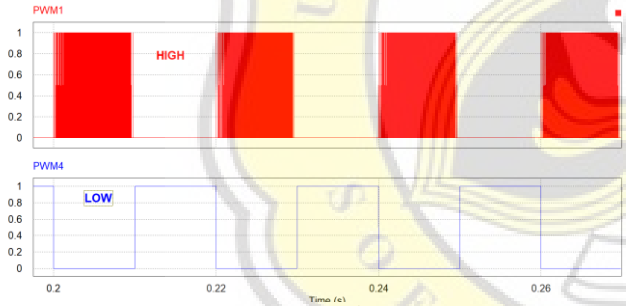


Fig 10. Switching simulation result PWM from inverter TPFW

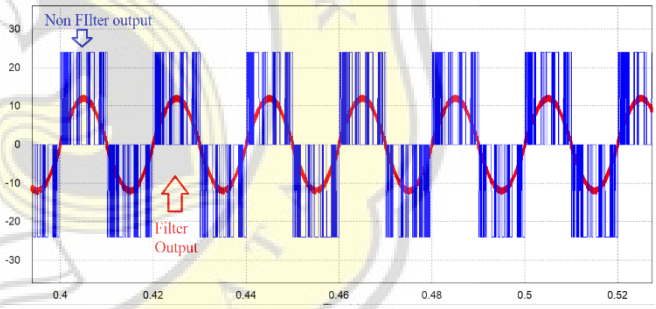


Fig 12. Result of simulation Non-filter output and Filtering output

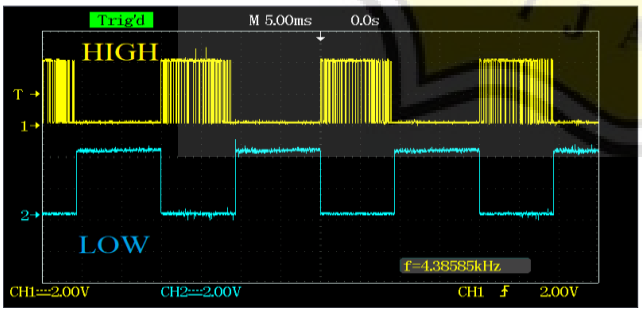


Fig 11. Switching hardware results in PWM from inverter TPFW

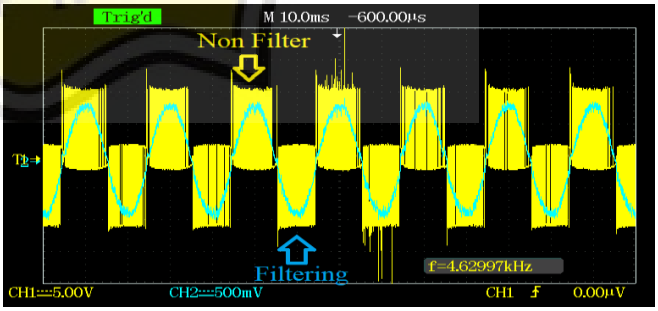


Fig 13. Result of implementation Non-filter output and Filtering output

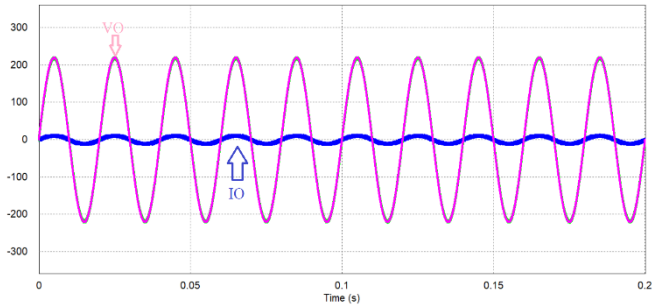


Fig 14. Result of simulation output voltage and output current

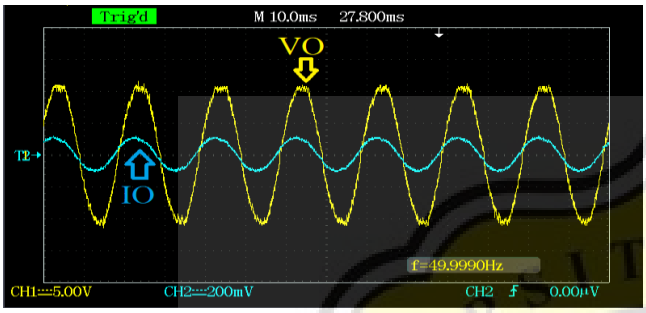


Fig 15. Result of hardware implementation output voltage and output current

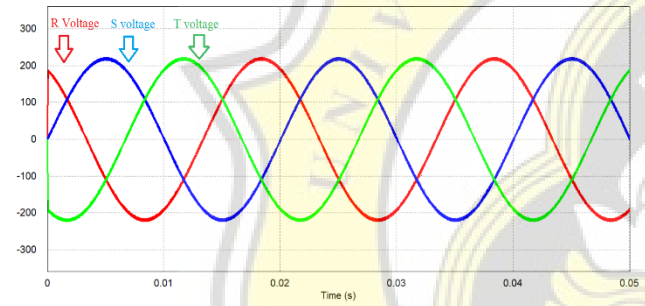


Fig 16. Result of simulation output voltage inverter TPFW double loop

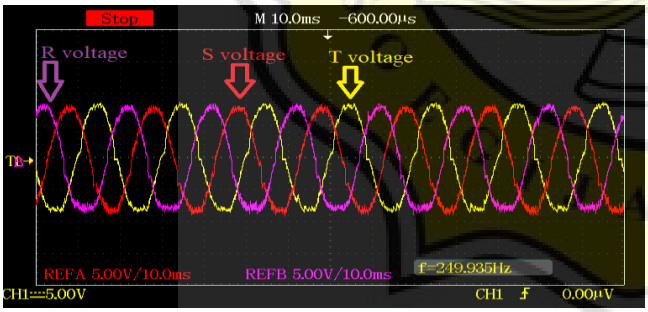


Fig 17. Result of implementation output voltage inverter TPFW double loop

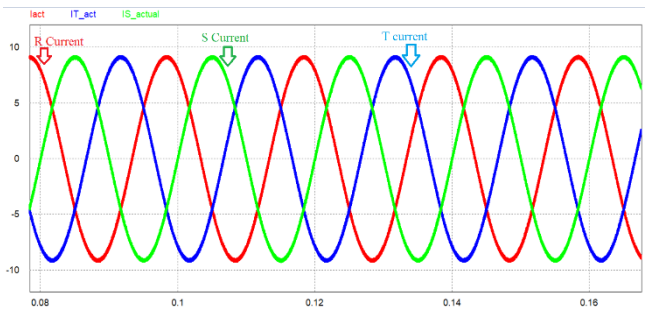


Fig 18. Result of simulation output current inverter TPFW double loop

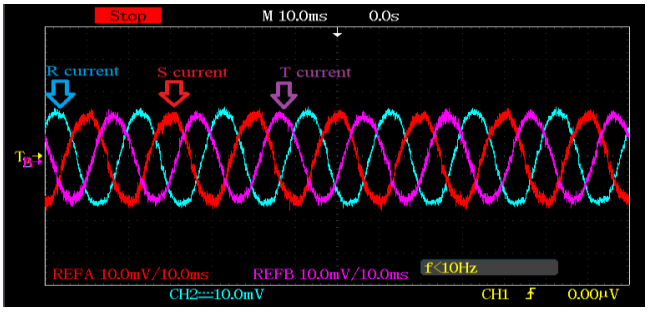


Fig 19. Result of implementation output current inverter TPFW double loop

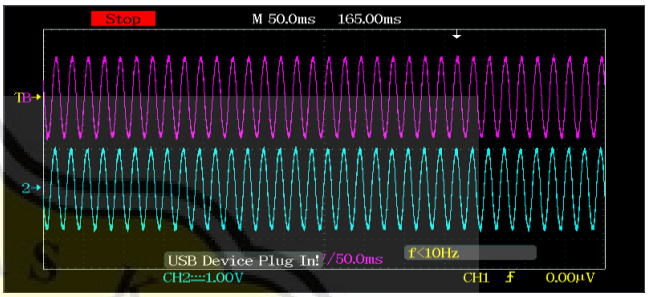


Fig 20. Result of implementation output voltage inverter with additional load and normal load

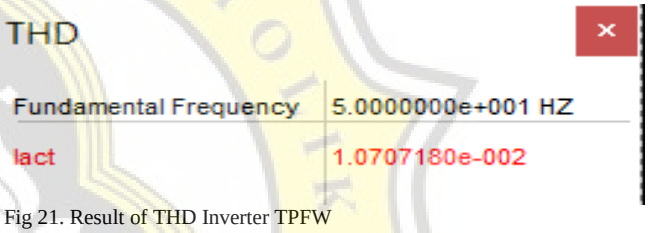


Fig 21. Result of THD Inverter TPFW

Fig. 10 and Fig. 11 show the gating signal on the power switching from the inverter double loop three-phase four-wired. From the Figure, we can see the high-frequency SPWM switching leg from part of high-power switches that operation of cycle switching making it unipolar operation mode for the inverter. For the low gating signal part of switching from Fig. 10 and Fig. 11 from the simulation and hardware implementation, the switching operated at a low–frequency based on the zero-crossing detector.

From part of high switching produced positive cycle and from part of low power, switches produce negative cycle for the inverter. There is a magnitude level voltage between 0 and +32V for the positive cycle and 0 to -32V for the negative cycle. The switching pattern generates a unipolar SPWM signal, which is then filtered by an inductor to produce a sinusoidal waveform, as seen in Fig. 12 and Fig. 13.

The output voltage (VO) and current (IO) generated by an inverter are displayed in Fig. 14 and Fig. 15. The output current signal is phase-locked to the voltage to the non-linear load, according to the flowchart program depicted in Fig. 9. Output voltage before filtering and after filtering, shown in Fig. 12 and Fig. 13, have been validated by hardware implementation. The output voltage of the inverter after thought step-up transformer produces 200 VPP alternating current with a load of 400 watts. A current of 4 amperes is obtained in each phase shown in Fig. 16 and Fig. 17. From the Figure, a neutral current that is close to 0 amperes, an angle of 0° has shown on the R phase voltage and current R,

then the angle of 120° shown on the S phase voltage and S phase current the angle 240° is shown on the T phase voltage and T phase current.

The output current of each phase is shown in Fig. 18 and Fig. 19. High THD value caused electrical equipment damage. Fig. 20 shows the result of implementation output voltage with the additional load. As we saw from the Figure, when the inverter has an additional load, the inverter does not cause a voltage drop. Based on further research from Fig. 21, the THD value can be generated by simulation by 1.07%.From the calculation $1.07e_{-002} \times 100\%=1.07\%$. From the result, the THD is less than 5% which corresponds with the standard IEEE 519.

IV. CONCLUSION

The simulation and implementation on hardware prove the double-loop control for a TPFW inverter. The SPWM power control design on the double-loop control TPFW inverter generates a stable sinusoidal waveform from the regulated output voltage and current, allowing for a slight reduction in switching loss and an increase in efficiency when compared to conventional active power switch inverters. According to the results, the double-loop control TPFW inverter does not cause distortion for the output voltage and current. The experiment is proven by changing the value of the load using a non-linear load. The output voltage and current maintain their shape and value given by the sinusoidal waveform reference.

This inverter is compatible with the power grid injection. This study established that the proposed strategy and control strategy makes a good result device suitable. This work is proven by the generated THD result, which has a value of 1.07% in accordance with the IEEE 519 harmonic standard. Furthermore, this proposed control strategy can be upgraded into a more advanced combination of control strategies, or this strategy can be implemented in a newly proposed topology.

ACKNOWLEDGMENT

This work was supported by the Directorate of Research and Community Service, Directorate General of Research Strengthening and Development, The Ministry of Research, Technology and Higher Education, Republic of Indonesia 2021.

REFERENCES

[1] P. N. Rao and J. Nakka, "Three-Phase Four-Leg Four-Wire Topology in High Power Factor Converter addressing the problem of unbalanced source currents," 2018 IEEE 8th Power India International Conference (PIICON), 2018, pp. 1-6, DOI: 10.1109/POWERI.2018.8704390I.

[2] A. A. Khan, U. A. Khan, H. F. Ahmed, H. Cha and S. Ahmed, "Improved NPC Inverters Without Short-Circuit and Dead-Time Issues," in IEEE Transactions on Power Electronics, vol. 37, no. 2, pp. 2180-2190, Feb. 2022, DOI: 10.1109/TPEL.2021.3103159.

[3] Y. Kihara, S. Hikosaka, H. Yamada, T. Tanaka, F. Ikeda, M. Okamoto, and S. R. Lee, "Harmonics Compensation with Constant DC-Capacitor Voltage-Control-Based Strategy for an Active Power-Line Conditioner in Three-Phase Four-Wire Distribution Feeders," 2020 23rd International Conference on Electrical Machines and Systems (ICEMS), 2020, pp. 971-976, DOI: 10.23919/ICEMS50442.2020.9291139

[4] Z. Zhu and W. Chen, "Zero sequence voltage and current control in four-wire grids-fed by grid-forming inverters," in CSEE Journal of Power and Energy Systems, DOI: 10.17775/CSEEJPES.2020.03230M.

[5] D. I. Brandao, F. E. G. Mendes, R. V. Ferreira, S. M. Silva, and I. A. Pires, "Active and Reactive Power Injection Strategies for Three-Phase Four-Wire Inverters During Symmetrical/Asymmetrical Voltage Sags," in IEEE Transactions on Industry Applications, vol. 55, no. 3, pp. 2347-2355, May-June 2019, DOI: 10.1109/TIA.2019.2893135.

[6] A. F. Wibisono and L. H. Pratomo, "Implementation of Voltage Control in Single-Phase Full Bridge Inverter Using One-Leg Plus Hysteresis Controller," 2021 International Conference on Technology and Policy in Energy and Electric Power (ICT-PEP), 2021, pp. 11-16, DOI: 10.1109/ICT-PEP53949.2021.9600987.

[7] L. H. Pratomo and C. Tjokro, "Hardware Implementation of an Asymmetrical 11-Level Inverter with Automatic Boost Charge Control in PV Applications," 2019 International Seminar on Application for Technology of Information and Communication (iSemantic), 2019, pp. 336-341, DOI: 10.1109/ISEMANTIC.2019.8884256.

[8] Z. Lin, X. Ruan, L. Jia, W. Zhao, H. Liu, and P. Rao, "Optimized Design of the Neutral Inductor and Filter Inductors in Three-Phase Four-Wire Inverter with Split DC-Link Capacitors," in IEEE Transactions on Power Electronics, vol. 34, no. 1, pp. 247-262, Jan. 2019, DOI: 10.1109/TPEL.2018.2812278.

[9] Y. Fu, Y. Li, Y. Huang, X. Lu, K. Zou, C. Chen, and H. Bai, "Imbalanced Load Regulation Based on Virtual Resistance of a Three-Phase Four-Wire Inverter for EV Vehicle-to-Home Applications," in IEEE Transactions on Transportation Electrification, vol. 5, no. 1, pp. 162-173, March 2019, DOI: 10.1109/TTE.2018.2874357.

[10] H. Moon, J. Lee, J. Lee, and K. Lee, "MPC-SVM method with subdivision strategy for current ripples reduction and neutral-point voltage balance in three-level inverter," 2017 IEEE Energy Conversion Congress and Exposition (ECCE), 2017, pp. 191-196, DOI: 10.1109/ECCE.2017.8095780.

[11] T. Qanbari and B. Tousi, "Single-Source Three-Phase Multilevel Inverter Assembled by Three-Phase Two-Level Inverter and Two Single-Phase Cascaded H-Bridge Inverters," in IEEE Transactions on Power Electronics, vol. 36, no. 5, pp. 5204-5212, May 2021, DOI: 10.1109/TPEL.2020.3029870.

[12] A. Tcai, S. Pugliese and M. Liserre, "Discontinuous Modulation of Interleaved Parallel NPC Inverters with Reduced Circulating Current," 2019 IEEE Energy Conversion Congress and Exposition (ECCE), 2019, pp. 4403-4408, DOI: 10.1109/ECCE.2019.8912174.

[13] S. He, D. Zhou, X. Wang, and F. Blaabjerg, "Grid Voltage Sensorless Control of Three-Phase LCL Grid-Connected Inverters Using Multisampled Current," 2020 IEEE 9th International Power Electronics and Motion Control Conference (IPEMC2020-ECCE Asia), 2020, pp. 2002-2006, DOI: 10.1109/IPEMC-ECCEAsia48364.2020.9367836.

[14] S. Jena, N. Tiwary, C. K. Panigrahi and P. K. Sahu, "Performance Improvement of Grid Integrated Voltage Source Inverter Using Different Hysteresis Current Controllers," 2020 IEEE 7th Uttar Pradesh Section International Conference on Electrical, Electronics and Computer Engineering (UPCON), 2020, pp. 1-6, DOI: 10.1109/UPCON50219.2020.9376436.

[15] L. H. Pratomo and S. Aditya, "Design and Implementation of One-Leg and PI Control Single-Phase H-Bridge Current Regulated Inverter," 2021 International Seminar on Application for Technology of Information and Communication (iSemantic), 2021, pp. 376-382, DOI: 10.1109/iSemantic52711.2021.9573251.

[16] S. K. Singh and S. Ghatak Choudhuri, "A conflict in control strategy of voltage and current controllers in Multi-Modular single-phase UPS inverters system," 2017 10th International Symposium on Advanced Topics in Electrical Engineering (ATEE), 2017, pp. 631-636, DOI: 10.1109/ATEE.2017.7905042.

[17] A. S. Mohamad, "Matrix Inverter: A Multilevel Inverter Based on Matrix Converter Switch Matrix," 2020 IEEE Electric Power and Energy Conference (EPEC), 2020, pp. 1-5, DOI: 10.1109/EPEC48502.2020.9320121.

[18] J. Baek, S. -E. Kim and S. Kwak, "Predictive control method for load current of single-phase voltage source inverters," 2015 IEEE Applied Power Electronics Conference and Exposition (APEC), 2015, pp. 2256-2260, DOI: 10.1109/APEC.2015.7104663.

[19] S. Fan, Y. Yu, Y. Zhang, and H. Yang, "Multi-mode Synchronized PWM Schemes for three-level NPC Inverter," 2019 22nd International Conference on Electrical Machines and Systems (ICEMS), 2019, pp. 1-5, DOI: 10.1109/ICEMS.2019.8921689.

[20] S. K. Singh and S. Ghatak Choudhuri, "A conflict in control strategy of voltage and current controllers in Multi-Modular single-phase UPS inverters system," 2017 10th International Symposium on Advanced Topics in Electrical Engineering (ATEE), 2017, pp. 631-636, DOI: 10.1109/ATEE.2017.7905042.

[21] Rajiv K. Varma, "Control Coordination of Smart PV Inverters," in Smart Solar PV Inverters with Advanced Grid Support Functionalities, IEEE, 2022, pp. 369-429, DOI: 10.1002/9781119214236.ch8.

[22] Rajiv K. Varma, "Emerging trends with smart solar PV inverters," in Smart Solar PV Inverters with Advanced Grid Support Functionalities, IEEE, 2022, pp. 431-464, DOI: 10.1002/9781119214236.ch9.

[23] Rajiv K. Varma, "Modeling and control of three-phase smart PV inverters," in Smart Solar PV Inverters with Advanced Grid Support Functionalities, IEEE, 2022, pp. 73-106, DOI: 10.1002/9781119214236.ch3.

[24] T. Qanbari and B. Tousi, "Single-Source Three-Phase Multilevel Inverter Assembled by Three-Phase Two-Level Inverter and Two Single-Phase Cascaded H-Bridge Inverters," in IEEE Transactions on Power Electronics, vol. 36, no. 5, pp. 5204-5212, May 2021, DOI: 10.1109/TPEL.2020.3029870.

[25] B. K. Gupta, K. R. Sekhar, and A. I. Gedam, "Balanced Per-Phase Sequential Switching to Suppress Circulating Current in Grid Connected Modular Solar Inverters," 2019 8th International Conference on Renewable Energy Research and Applications (ICRERA), 2019, pp. 686-691, DOI: 10.1109/ICRERA47325.2019.8996838.

[26] H. Jiang, Y. Zhang, L. Huang, and J. Liu, "An Inverter Input Current Closed-loop Control Scheme for IPMSM Drives Fed by Electrolytic Capacitorless Converter," 2020 IEEE 9th International Power Electronics and Motion Control Conference (IPEMC2020-ECCE Asia), 2020, pp. 1795-1799, DOI: 10.1109/IPEMC-ECCEAsia48364.2020.9367930.

[27] G. D. O. Assuncao and I. Barbi, "Method for Deriving Transformerless Common-Ground Voltage Source Inverter Topologies," in IEEE Transactions on Power Electronics, DOI: 10.1109/TPEL.2022.3162771.

[28] "IEEE Draft Standard for Interconnection and Interoperability of Inverter-Based Resources (IBR) Interconnecting with Associated Transmission Electric Power Systems," in IEEE P2800/D6.1, June 2021, vol., no., pp.1-197, 11 June 2021.

[29] H. Jiang, Y. Zhang, L. Huang, and J. Liu, "An Inverter Input Current Closed-loop Control Scheme for IPMSM Drives Fed by Electrolytic Capacitorless Converter," 2020 IEEE 9th International Power Electronics and Motion Control Conference (IPEMC2020-ECCE Asia), 2020, pp. 1795-1799, DOI: 10.1109/IPEMC-ECCEAsia48364.2020.9367930.

[30] A. Panda, G. Dyanamina and R. K. Singh, "MATLAB Simulation of Space Vector Pulse Width Modulation for 3-level NPC Inverter and 2-level Inverter," 2021 International Conference on Sustainable Energy and Future Electric Transportation (SEFET), 2021, pp. 1-5, DOI: 10.1109/SeFet48154.2021.9375668.