

The Voltage Control in Single-Phase Five-Level Inverter for a Stand-Alone Power Supply Application

Daniel Santoso¹, Leonardus Heru Pratomo²

^{1,2}Department of Electrical Engineering, Soegijapranata Catholic University, Semarang, Indonesia
 Email: ¹santosodaniel4@gmail.com, ²leonardus@unika.ac.id

Abstract— Inverters have been widely used since more devices require alternating current (AC) voltage source. However, these devices require a stable AC voltage source, so that the device is not easily damaged. The solution is to control the inverter output voltage to be applied as a standalone power supply. The main problem is that standalone power supplies generally use conventional inverters. Conventional inverters require high switching frequencies and large inductance filters so that harmonic distortion at undesirable voltages that affect the durability of electrical equipment does not exceed the IEEE 519 standard. The purpose of this research is to provide a solution using a single-phase five-level inverter for stand-alone power supply applications. This research method applies a new control strategy on sinusoidal pulse width modulation (SPWM) to control the output voltage of a single-phase five-level inverter. The SPWM signal is generated by comparing two sinusoidal reference signals that are shifted 180 degrees with two cascaded carrier signals. This research has been verified by simulating, implementing, and testing the THD voltage in the laboratory. As a result, the output voltage of the five-phase single-phase inverter has been controlled based on the reference voltage with a voltage THD value of 4.39%. This meets the standard THD voltage from IEEE 519 below 5%, so it can be applied as a stand-alone power supply. Another advantage, this inverter uses an asymmetric topology with fewer power switches compared to other topologies of five-level inverters.

Keywords— Five-level inverter, asymmetric, stand-alone power supply, THD.

I. INTRODUCTION

The research of inverter technology is continuing in the era of digital transformation [1]–[3]. Hence, in the era of digital transformation, many devices use AC sources [4], [5]. The main problem is that many devices that use AC sources require a controlled AC voltage source based on the standard THD voltage from IEEE 519 so that the device is not easily damaged [6]–[8]. A stand-alone power supply is a solution because it can produce a controlled AC voltage as desired [9]. A stand-alone power supply usually using a conventional inverter [10]. Conventional inverters use a high switching frequency so that they require a large inductor filter to get a low defective voltage level on the output side is a problem in this case [11]. The multilevel inverter is used as standalone power supplies to solve the problem because it can be operated at low switching frequencies [12].

Research on power inverters used to reduce harmonics is by using multilevel inverter technology without having to use

large inductor filters [13], [14]. In general, multilevel inverters do not require large inductor filters to produce low harmonics because the SPWM switching frequency is low [15]. A single-phase multilevel inverter which exists is divided into three types such as cascade, diode clamped, and flying capacitor [16], [17]. A single-phase five-levels with the cascade topology has eight power switches [18]. The new research of cascaded a single-phase five-level inverter has six power switches [19]. In a single-phase five-levels with flying capacitor topology using eight power switches [20]. The new research of the flying capacitor which uses hybrid methods (combined with another topology) has six power switches [21].

A asymmetric single-phase multilevel inverter is used to resolve that problem [22]. The asymmetric method provides a voltage value which is different for every amount input source [23]. The asymmetric type five-level inverter has the advantages that the amount of switches used less than other five-level inverters so that it has a simpler switching and is easier to control [24], [25]. This asymmetric five-level inverter uses a zero-crossing detector to correct unbalanced signal forms (spikes/sags between positive and negative cycles) so that the system becomes more stable [26].

The purpose of this research is to produce a single-phase five-level inverter for stable stand-alone power supply applications. A stable stand-alone power supply is made by applying a proportional-integral (PI) control to controlling the output voltage of a single-phase five-stage inverter [27]. The single-phase five-level inverter uses a new control strategy in the sinusoidal pulse width modulation (SPWM) method such as described in section 2. The advantage of this research method is that the number of power switches used is less than the single-phase five-level inverter with other types of topology. In section 3, verification of this strategy is carried out by simulation and testing of the hardware in the laboratory. In section 4, the hardware implementation results produce an output voltage that is compared to the THD standard voltage from IEEE 519. This research is important to develop because there are so many devices in the industry and others that require a stand-alone power supply as a stable AC voltage source so that these devices are not easily damaged by voltage harmonics.



II. RESEARCH METHODS

This research uses a method such as the flow chart shown in Figure 1. The research method is carried out by reviewing the literature, identifying existing problems, simulation, hardware implementation, testing, and concluding based on the test results. The research started by learning the literature related to the five-level single-phase inverter. Based on this literature, several problems were identified. The first solving of a problem in a five-level inverter is simulated using Power Simulator (PSIM) software to verify the method. Simulation verified by hardware implementation in laboratory. Each simulation and implementation are tested and retrieval the data. In the final stage, THD will be tested in order to produce conclusions. The conclusions obtained will be used to overcome this problem.

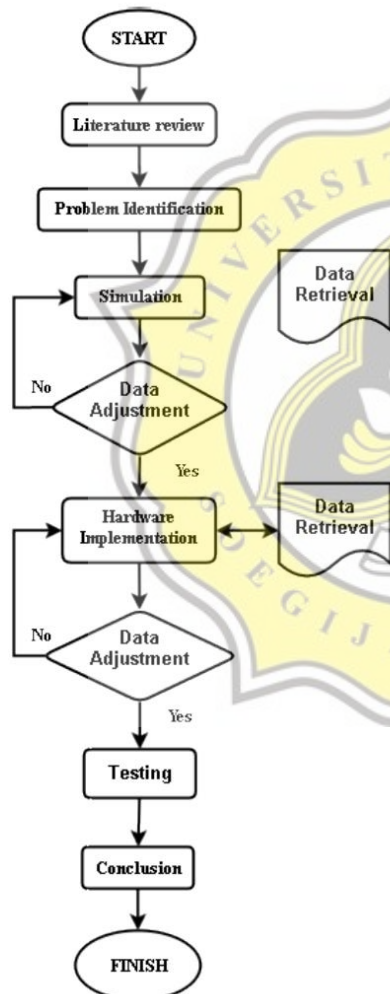


Fig. 1. Research method flow chart

The new research of asymmetric single-phase five-level has five power switches (S1-S5) as shown in Figure 2 [28]. This inverter requires two separate DC sources (E). The diode (D1) in the asymmetric single-phase five-level inverter is operated in forwarding bias. At the end of the output of the five-level inverter is given an inductor filter (L), before going to the load (R). The output voltage of the inverter measured at the load is called VO.

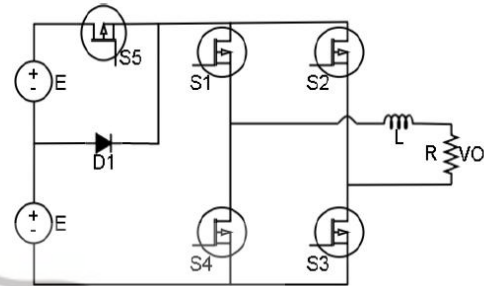


Fig. 2. Asymmetric single-phase five-level inverter topology

A. Five-Level Inverter Operation Mode

This five-level single-phase inverter has five modes of operation [29]. In the first mode of operation the power switches (S5), (S1) and (S3) are energized. In the second mode of operation both the power switches (S1) and (S3) are energized. The third mode of operation is the freewheeling condition. In the fourth mode of operation the both power switches (S2) and (S4) are energized. In the fifth mode of operation the power switches (S5), (S2) and (S4) are energized.

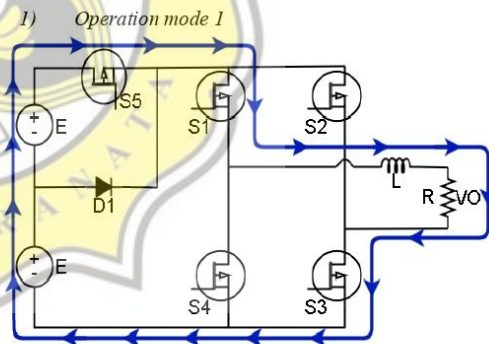


Fig. 3. Operation mode 1

When power switches S5 and S1 are induced by current, current flows from the DC source (E + E) to the load. When current induces power switch S4, current flows back to the DC source (E + E). Operation mode 1 is illustrated in Figure 3. The equation for operation mode 1 is represented in (1). This voltage equation explains that the inverter input voltage of 2E is the sum of the voltage on the inductance filter (VL) and the inverter output voltage (VO).

$$2E = V_{(L)} + V_{(o)} \tag{1}$$

2) Operation mode 2

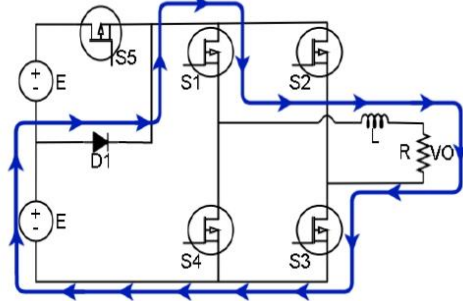


Fig. 4. Operation mode 2

When the power switch S1 and the diode D0 are induced by current, current flows from the DC source (E) to the load. When the power switch S3 is induced by the current, the current flows back to the DC source (E). Operation mode 2 is illustrated in Figure 4. The equation for operation mode 2 is represented in (2). This voltage equation explains that the inverter input voltage of E is the sum of the voltage on the inductance filter (VL) and the inverter output voltage (VO).

$$E = V_{(L)} + V_{(o)} \tag{2}$$

3) Operation mode 3

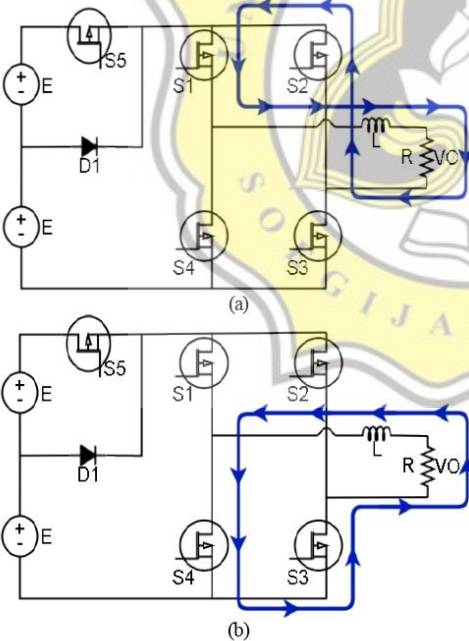


Fig. 5. Operation mode 3. (a) Positive Cycle. (b) Negative Cycle

$$V_{(L)} + V_{(o)} = 0 \tag{3}$$

In this mode is freewheeling. There are two stages of the freewheeling condition, which are a positive cycle and a negative cycle. After the current flows on the power switches S1 and S3, freewheeling occurs on the positive cycle. After the current flows on the power switches S2 and S4, freewheeling occurs on the negative cycle. Operation mode 3 is illustrated in Figure 5 (a). Positive cycle. Figure 4 (b). Negative cycle. This voltage equation explains that the sum of the voltage on the inductance filter (VL) and the inverter output voltage (VO) is 0. The equation for mode of operation 3 is represented in (3).

4) Operation Mode 4

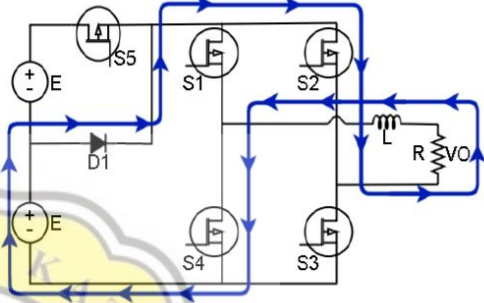


Fig. 6. Operation mode 4

When power switch S2 and the diode D0 are induced by a current, current flows from the DC source (E) to the load. When current induces power switch S4, current flows back to the DC (E) source. Operation mode 4 is illustrated in Figure 6. The equation for operation mode 4 is represented in (4). This voltage equation explains that the inverter input voltage of -E is the sum of the voltage on the inductance filter (VL) and the inverter output voltage (VO).

$$-E = V_{(L)} + V_{(o)} \tag{4}$$

5) Operation Mode 5

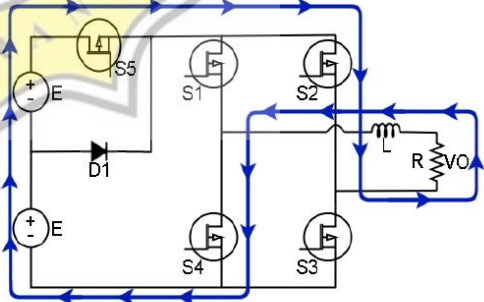


Fig. 7. Operation mode 5

When the power switch S5 and S2 are induced by the current, current flows from the DC source (E + E) to the load. When the power switch S4 is induced by current, the current flows back to the DC source (E + E). Operation mode 5 is illustrated in Figure 7.

The equation for operation mode 5 is represented in (5). This voltage equation explains that the inverter input voltage of $2E$ is the sum of the voltage on the inductance filter (V_L) and the inverter output voltage (V_O).

$$-2E = V_L + V_O \tag{5}$$

According to the mode of operation (1-5), a switching table for each power switch is obtained as shown in Table 1.

TABLE I. SPWM GATE SWITCHING

S1	S2	S3	S4	S5	VO
1	0	1	0	1	2E
1	0	1	0	0	E
1	0	0	0	0	0
0	0	0	1	0	0
0	1	0	1	0	-E
0	1	0	1	1	-2E

B. The Stand-Alone Control Strategy

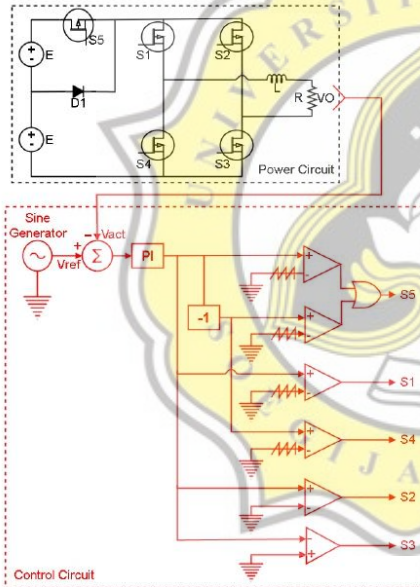


Fig. 8. Power circuit along with five-level inverter control circuit

The Stand-Alone Control Strategy is divided into two parts, which are the power circuit and the control circuit. The power circuit consists of five power switches such as (S1-S5), one power switch that functions as a diode (D1), two separate DC sources for each voltage of E , inductor filter (L), and load (R). The SPWM signal on each power switch is obtained from the control circuit. The control circuit uses a reference signal in the form of a sinusoidal signal and an actual signal from the voltage sensor was reading.

The reference signal is subtracted from the actual signal to produce an error signal. The error signal is entered into the PI control to produce a PI signal. The PI signal is multiplied by -1 to get a MIN signal that is shifted by 180 degrees. PI and MIN signals as reference are modulated with the carrier signal through the comparator circuit in the control circuit to produce SPWM signals for each power switch. The power and control circuit schematic is shown in Figure 8.

The single-phase five-level inverter is programmed using the Arduino Due microcontroller. The programming algorithm begins by reading the reference signal and reading the actual signal from the inverter output voltage. Then the reference signal is subtracted from the actual signal and entered into the PI control. The PI value that was shifted by 180° was initialized with MIN. If the value of PI is greater than $car1$ then S1 has logic 1. If the MIN value is greater than $car1$ then S4 has logic 1. If the PI value is greater than $car2$ then A will have logic 1. If the MIN value is greater than $car2$ then B will have logic 1. Otherwise, S1, S4, A, and B will have logic 0. The result of A or B is S5. The values greater than the limit of 0 are initialized as offset. If the PI value is greater than the offset value, S3 has logic 1 and S2 has logic 0. If the PI value is less than the offset value, so the S3 will have logic 0 and S2 has logic 1. The programming algorithm is shown in Figure 9.

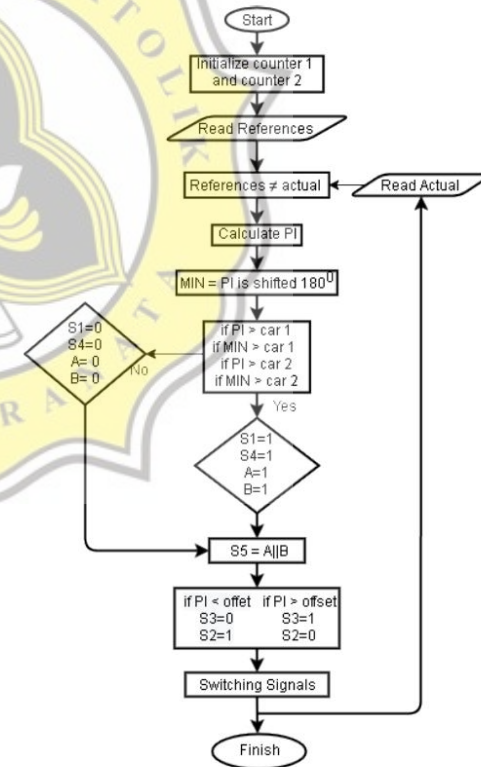


Fig. 9. Programming algorithm

III. RESULT AND DISCUSSION

Voltage control on a single-phase five-level inverter has been simulated in the Power Simulator software. The simulation parameters are shown in Table 2.

TABLE II. THE SIMULATION PARAMETERS

Parameter	Value
DC Source (E)	35 V
Inductance Filter	2 mH
Load	60Ω
Carrier signal frequency	5 KHz

Figure 10 shows the SPWM signal on each power switch. SPWM is applied using two reference signals. The first reference signal is PI. The PI phase was shifted to 180, a second reference signal (MIN) was obtained. PI and MIN signals are modulated with two carrier signals, it is car1 and car2. The carrier signal used is a triangular wave signal and has a frequency of 5 KHz. The carrier signal used is a triangular wave signal and has a frequency of 5 kHz. The first carrier signal (car1) is on the first level and the carrier signal (car2) on the second because they have different DC offsets. Power switch S1 known as high (H1) and S2 as H2 cannot be active simultaneously. The power switch S4 known as low (L1) and S3 as L2 also do not turn on simultaneously. Likewise, for H1 and L1, both of them should not be active at the same time as H2 and L2. They don't turn on at the same time in each cycle, 2E, E, 0, 0, -E, -2E.

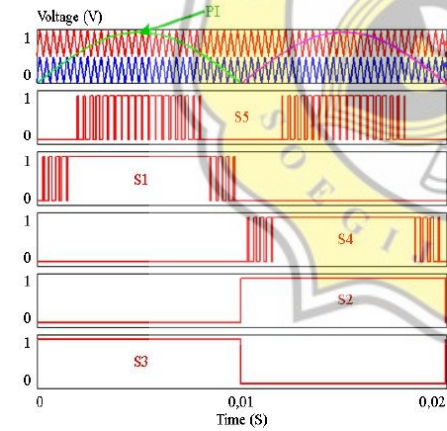


Fig. 10. SPWM signal on each power switch

The success parameter of controlling the output voltage on the asymmetric single-phase five-level inverter is seen in the actual signal generated. Figure 11 shows the simulation results of the actual signal (Vact) following the reference signal (Vref). This proves that the output voltage of the asymmetric single-phase five-stage inverter has been successfully controlled. So it can be used for stand-alone power supply applications as a stable voltage source.

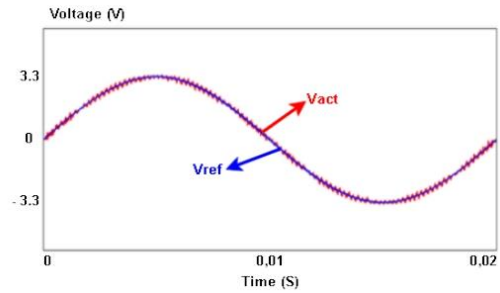


Fig. 11. The results comparison of actual (Vact) and reference (Vref)

The simulation results were successfully carried out by displaying five levels of stress. Five voltage levels are displayed by measuring the voltage at the input inductance filter (VL). While the measurement results of the output voltage at the load generate a VO signal. The simulation results for VL and VO signals are shown in Figure 12.

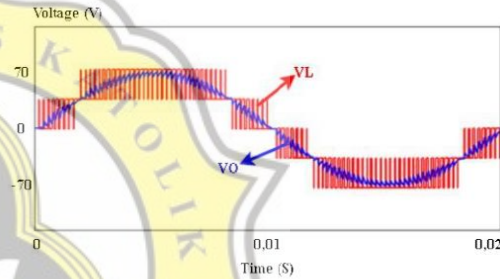


Fig. 12. Inverter output signal before filter (VL) and after filtering (VO)

The output current of the asymmetric single-phase five-level inverter is shown by placing a current meter in series between the inverter output and the inductor filter. The current generated by the asymmetric single-phase five-level inverter is initialized with IO. The simulation results for VO and IO are shown in Figure 13.

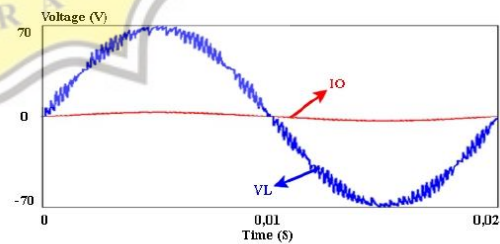


Fig. 13. Inverter output signal VO and IO

A. The Implementation Results in the Laboratory

Figure 14 shows the implementation of an asymmetric single-phase five-level inverter in the laboratory. This implementation is to verify the results of simulation. Implementation data are taken using an oscilloscope. The implementation parameters are shown in Table 3.

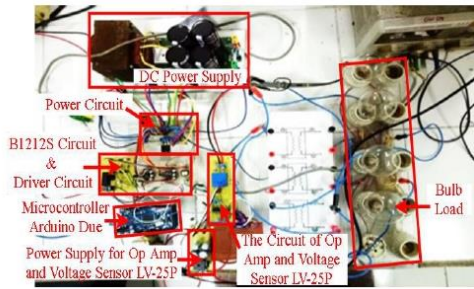


Fig. 14. Hardware implementation

TABLE III. THE IMPLEMENTATION PARAMETERS

Parameter	Value
DC Source (E)	35 V
Inductance Filter	2 mH
Bulb Load	100 Watt
Carrier signal frequency	5 KHz

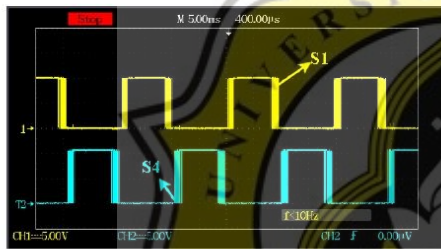


Fig. 15. Data from oscilloscope for S1 and S4

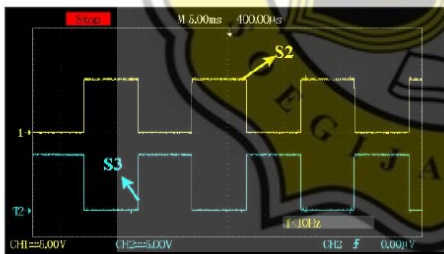


Fig. 16. Data from oscilloscope for S2 and S3

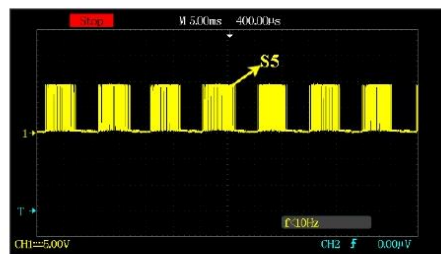


Fig. 17. Data from oscilloscope for S5

Figure 15 shows the SPWM switching for power switches at the S1 and S4. The SPWM for power switches S2 and S3 is shown in Figure 16. The SPWM for power switches S5 is shown in Figure 17.

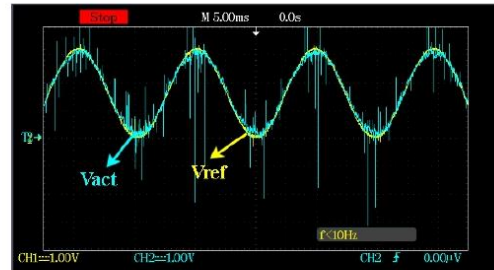


Fig. 18. The results of measuring Vact and Vref signals using an oscilloscope

The results of measurements using an oscilloscope on a single-phase five-level inverter implemented in the laboratory show that the actual voltage (Vact) always follows the reference voltage (Vref) and is shown in Figure 18. Figure 18 has verified the simulation results in Figure 11. Hence, the asymmetric single-phase five-level inverter can be used for a stand-alone power supply as a stable voltage source.



Fig. 19. The results of measuring VL and VO signals using an oscilloscope

Figure 19 shows the output voltage before filtering (VL) and the output voltage after filtering (VO). Figure 19 has verified the simulation results from Figure 12. Figure 20 displays the output voltage (VO) and the inverter output current (IO). Figure 20 has verified the simulation results from Figure 13.

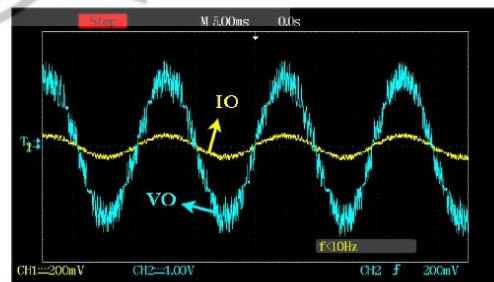


Fig. 20. The results of measuring VO and IO signals using an oscilloscope

Based on the simulation and implementation results, control of the five-level inverter output voltage is running well. This is evidenced by measuring the THD voltage value using the HIOKI 3286-20 THD power meter record function. Figure 21 shows the THD measurement results of 4.39%.

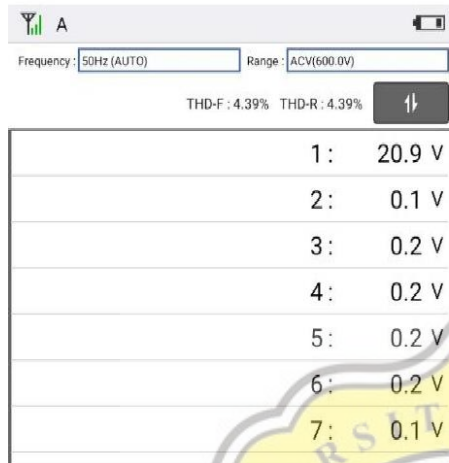


Fig. 21. The measurement result of the THD value

In general, inverters used in standalone power supply systems are conventional inverters with high frequency and large inductance filters to obtain a low voltage THD. The solution is to use a multilevel inverter for standalone power supply applications [30]. The advantage of this study compared to similar studies is that it uses an asymmetric five-level single-phase inverter with a smaller number of power switches. Based on the test results, the output voltage of the asymmetrical single-phase five-level inverter has been controlled and can be used for stable stand-alone power supply based on the IEEE 519 voltage THD standard (Below 5% for 2.3 - 69kV usage).

IV. CONCLUSION

The five-level inverter with five power switches has been simulated and verified by implementation in the laboratory. The SPWM control design on an asymmetric five-level single-phase inverter produces an actual voltage that has followed the reference voltage. This proves that the control strategy that has been implemented can be running well. Based on these results, the asymmetric five-level single-phase inverter can be applied as a stable independent power supply with a voltage THD value of 4.39% based on the IEEE 519 harmonic standard.

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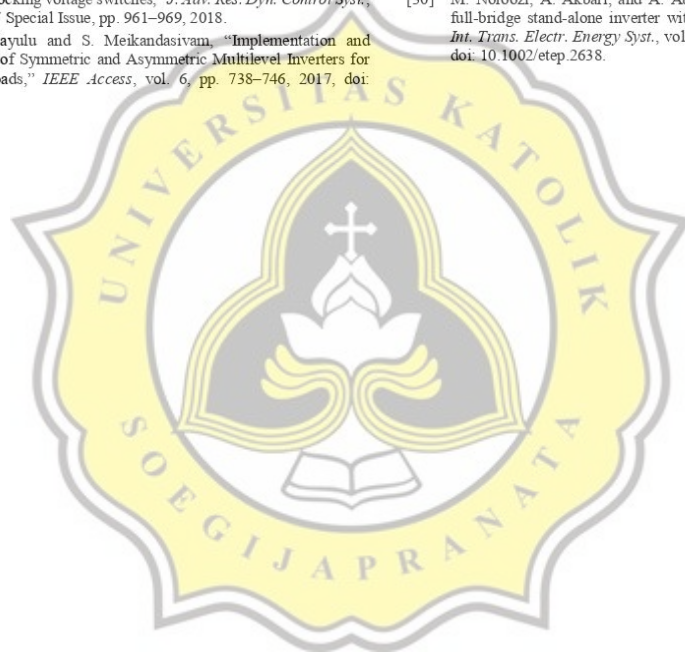
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REFERENCES

- [1] C. Tjokro and L. H. Pratomo, "Design and Simulation of an

- Asymmetrical 11-Level Inverter for Photovoltaic Applications," in *2018 5th International Conference on Information Technology, Computer, and Electrical Engineering (ICITACEE)*, Sep. 2018, pp. 93–98, doi: 10.1109/ICITACEE.2018.8576943.
- [2] J. L. Torre, L. A. M. Barros, J. L. Afonso, and J. G. Pinto, "Development of a Proposed Single-Phase Series Active Power Filter without External Power Sources," *SEST 2019 - 2nd Int. Conf. Smart Energy Syst. Technol.*, 2019, doi: 10.1109/SEST.2019.8849010.
- [3] H. Xu, Y. Peng, and L. Su, "Research on Open Circuit Fault Diagnosis of Inverter Circuit Switching tube Based on Machine Learning Algorithm," *IOP Conf. Ser. Mater. Sci. Eng.*, vol. 452, no. 4, p. 042015, Dec. 2018, doi: 10.1088/1757-899X/452/4/042015.
- [4] D. Setiawan, H. Eteruddin, and A. Arlemy, "Desain dan Analisis Inverter Satu Fasa Berbasis Arduino Menggunakan Metode SPWM," *J. Tek.*, vol. 13, no. 2, pp. 128–135, 2019, doi: 10.31849/teknik.v13i2.3491.
- [5] A. Algaddafi, K. Elnaddab, A. Al Ma'Mari, and A. N. Esgiar, "Comparing the performance of bipolar and unipolar switching frequency to drive DC-AC Inverter," *Proc. 2016 Int. Renew. Sustain. Energy Conf. IRSEC 2016*, no. October 2017, pp. 680–685, 2017, doi: 10.1109/IRSEC.2016.7984067.
- [6] L. P. S. Raharja, O. A. Q., Z. Arnef, and N. A. Windarko, "Reduction of Total Harmonic Distortion (THD) on Multilevel Inverter with Modified PWM using Genetic Algorithm," *Emit. Int. J. Eng. Technol.*, vol. 5, no. 1, pp. 91–118, Jul. 2017, doi: 10.24003/emitter.v5i1.174.
- [7] D. V. N. Ananth, "Power quality conditioning using series active power filter to compensate flickering and unbalanced loads Power quality conditioning using series active power filter to compensate flickering and unbalanced loads," no. April, 2018, [Online]. Available: <https://www.researchgate.net/publication/324605263%0APower>.
- [8] C. Jena, S. Mohapatra, S. Mishra, B. Panda, and A. Majumdar, "Power Quality Improvement by Reduction of Total Harmonic Distortion (THD) using PWM Inverter," *Int. J. Innov. Technol. Explor. Eng.*, vol. 9, no. 2, pp. 1641–1643, 2020, doi: 10.35940/ijitee.a5081.129219.
- [9] S. Mahajan, S. K. Subramaniam, K. Natarajan, A. G. Nanjappa Gounder, and D. V. Borru, "Analysis and control of induction generator supplying stand-alone AC loads employing a Matrix Converter," *Eng. Sci. Technol. an Int. J.*, vol. 20, no. 2, pp. 649–661, 2017, doi: 10.1016/j.jestech.2017.02.006.
- [10] J.-U. Lim, H.-W. Kim, K.-Y. Cho, and J.-H. Bae, "Stand-Alone Microgrid Inverter Controller Design for Nonlinear, Unbalanced Load with Output Transformer," *Electronics*, vol. 7, no. 4, p. 55, Apr. 2018, doi: 10.3390/electronics7040055.
- [11] E. Engineering, "Review of Inverter and Multilevel Inverter : Features , Techniques , Topology and Latest Developments," vol. 118, no. 24, pp. 1–12, 2018.
- [12] M. Ahmad and S. Kirmani, "Harmonics analysis of a SPV based stand-alone and grid connected multilevel inverter with improved power quality at different load," *Int. J. Sci. Technol. Res.*, vol. 8, no. 10, pp. 152–160, 2019.
- [13] N. Prabaharan and K. Palanisamy, "A comprehensive review on reduced switch multilevel inverter topologies, modulation techniques and applications," *Renew. Sustain. Energy Rev.*, vol. 76, no. April, pp. 1248–1282, Sep. 2017, doi: 10.1016/j.rser.2017.03.121.
- [14] M. S. Bhaskar, S. Padmanaban, V. Fedak, F. Blaabjerg, and P. Wheeler, "Transistor Clamped Five-Level Inverter using Non-Inverting Double Reference Single Carrier PWM Technique for photovoltaic applications," in *2017 International Conference on Optimization of Electrical and Electronic Equipment (OPTIM) & 2017 Intl Aegean Conference on Electrical Machines and Power Electronics (ACEMP)*, May 2017, pp. 777–782, doi: 10.1109/OPTIM.2017.7975063.
- [15] L. H. Pratomo and C. Tjokro, "Hardware Implementation of an Asymmetrical 11-Level Inverter with Automatic Boost Charge Control in PV Applications," in *2019 International Seminar on Application for Technology of Information and Communication (ISemantic)*, Sep. 2019, pp. 336–341, doi: 10.1109/ISEMANTIC.2019.8884256.
- [16] G. Mohapatra, "Multilevel inverter; A review MULTILEVEL INVERTER; A REVIEW," no. April, 2018.
- [17] K. Esakkishenbaga Loga and S. P. Umaya, "Multilevel Inverter Topology with Reduced Number of Switches," *Int. J. Eng. Adv.*

- Technol.*, vol. 8, no. 6S3, pp. 1730–1733, Nov. 2019, doi: 10.35940/ijeat.F1325.0986S319.
- [18] K. S. C. Mauryan and G. N. Institutions, "Design of Five-Level Cascaded H-Bridge Multilevel Inverter Design of Five-Level Cascaded H-Bridge Multilevel Inverter," no. July, 2020, doi: 10.1007/978-981-15-2256-7.
- [19] Y. Adem, "Design and Simulation of Single-Phase Five-Level Symmetrical Cascaded H-Bridge Multilevel Inverter with Reduces Number of Switches," *J. Electr. Electron. Syst.*, vol. 07, no. 04, 2018, doi: 10.4172/2332-0796.1000281.
- [20] S. Modugu, "Spwm techniques in five level inverter," no. December, 2018.
- [21] S. Khadse, R. Mendole, and A. Pandey, "A 5-Level Single Phase Flying Capacitor Multilevel Inverter," *Int. Res. J. Eng. Technol.*, vol. 4, no. 2, pp. 348–352, 2017, [Online]. Available: <https://irjet.net/archives/V4/i2/IRJET-V4I269.pdf>.
- [22] S. Mukherjee, S. De, S. Sanyal, S. Das, and S. Saha, "A 15-level asymmetric H-bridge multilevel inverter using d-SPACE with PDPWM technique," *Int. J. Eng. Sci. Technol.*, vol. 11, no. 1, p. 22, 2018, doi: 10.4314/ijest.v11i1.3.
- [23] K. Malik, S. Dora, S. George Fernandez, and K. Vijayakumar, "A new symmetric and asymmetric multilevel inverter topology with reduced maximum blocking voltage switches," *J. Adv. Res. Dyn. Control Syst.*, vol. 10, no. 7 Special Issue, pp. 961–969, 2018.
- [24] C. Dhananjayulu and S. Meikandasivam, "Implementation and Comparison of Symmetric and Asymmetric Multilevel Inverters for Dynamic Loads," *IEEE Access*, vol. 6, pp. 738–746, 2017, doi: 10.1109/ACCESS.2017.2775203.
- [25] S. Yousofi-Damian and S. Masoud Barakati, "A New Asymmetric Multilevel Inverter With Reduced Number of Components," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 8, no. 4, pp. 4333–4342, Dec. 2020, doi: 10.1109/JESTPE.2019.2945757.
- [26] P. Boucaud, F. De Soto, J. Rodriguez-Quintero, and S. Zafeiropoulos, "Refining the detection of the zero crossing for the three-gluon vertex in symmetric and asymmetric momentum subtraction schemes," *Phys. Rev. D*, vol. 95, no. 11, p. 114503, Jun. 2017, doi: 10.1103/PhysRevD.95.114503.
- [27] S. Ashikin Azmi, G. Philips Adam, and S. R. Abdul Rahim, "Voltage-controlled of a three-phase current source inverter in islanded operation," *Indones. J. Electr. Eng. Comput. Sci.*, vol. 16, no. 1, p. 156, 2019, doi: 10.11591/ijeecs.v16.i1.pp156-164.
- [28] L. H. Pratomo, "One Leg Control Strategy in Single-Phase Five-Level Inverter," in *2019 International Symposium on Electrical and Electronics Engineering (ISEE)*, Oct. 2019, pp. 216–220, doi: 10.1109/ISEE2.2019.8921072.
- [29] D. Santoso and L. Heru Pratomo, "Design and simulation of an asymmetrical control strategy in single-phase five-levels inverter," *J. Phys. Conf. Ser.*, vol. 1444, no. 1, p. 012029, Jan. 2020, doi: 10.1088/1742-6596/1444/1/012029.
- [30] M. Noroozi, A. Akbari, and A. Abrishamifar, "A 5-level modified full-bridge stand-alone inverter with reduced number of switches," *Int. Trans. Electr. Energy Syst.*, vol. 28, no. 12, p. e2638, Dec. 2018, doi: 10.1002/etep.2638.





4.75% PLAGIARISM
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BAB IPENDAHULUAN Latar Belakang Penelitian teknologi inverter terus berkembang di era transformasi digital [1]. Pada era transformasi digital banyak peralatan yang menggunakan sumber AC. Peralatan yang menggunakan sumber AC memerlukan tegangan sumber yang dapat dikendalikan dan memiliki nilai Total Harmonic Distortion (THD) tegangan sesuai standar IEEE 519. Sistem catu daya mandiri digunakan sebagai sumber AC yang dapat mengendalikan tegangan keluaran sesuai keinginan [2]. Sistem catu daya mandiri biasanya menggunakan inverter konvensional [3]. Inverter konvensional memiliki nilai THD yang tinggi karena pensaklaran pada inverter konvensional bekerja pada frekuensi rendah dan tidak menggunakan Sinusoidal Pulse Width Modulation (SPWM) [4]. Sistem catu daya mandiri pada photovoltaic biasanya menggunakan inverter bertingkat [5]. Hal ini dikarenakan inverter bertingkat memiliki nilai THD tegangan yang memenuhi standar IEEE 519. Inverter bertingkat pada umumnya memiliki pensaklaran yang rumit sehingga lebih sulit dikendalikan. Inverter bertingkat satu fasa yang sudah ada dibagi menjadi tiga macam yaitu cascaded, diode clamped, flying capacitor [6]. Inverter lima tingkat satu fasa dengan topologi cascaded memiliki delapan buah saklar daya [7]. Pengembangan inverter lima tingkat satu fasa tipe cascaded memiliki enam buah saklar daya [8]. Inverter lima