Design and Implementation of Inverter Single Phase Nine-Level Using PIC18F4550

Natanael Novalutfi Prasetiyo
Department of Electrical Engineering
Soegijapranata Catholic University
Semarang, Indonesia
natanaelnovalutfiprasetiyo@gmail.com

Leonardus Heru Pratomo *Department of Electrical Engineering*
Soegijapranata Catholic University
Semarang, Indonesia
leonardus_hp@yahoo.com

***Abstract*—Multilevel inverters have been widely accepted for high-power, high-voltage applications. This paper proposes a multilevel inverter (MLI) topology with the combination of four buck DC-DC converters and H-Bridge inverter to produce a nine-level inverter. The four buck DC-DC converter operates with high frequency for generating voltage levels and H-bridge inverter with low frequency (50 Hz) operates for reversing the polarity of the output. The controlling technique was done digitally using PIC18F4550 to simplify control strategy. Finally, a prototype of the nine-level proposed topology is built and tested to show the performance of the inverter by experimental results.**

Keywords—Nine-level, Inverter, PIC18F4550

I. INTRODUCTION

Multilevel inverters (MLI) are investigated to fulfill the necessity of pure sinusoidal waveforms, with fewer harmonic distortion contents. The renewable energy sources are becoming popular in exchange of fuel sources and their disadvantages to the environment. The use of renewable energy is expected to rise every year [1]. Photovoltaic (PV) is the recommended renewable energy [2]. The universal MLI is known as cascaded H-bridge inverters, flying capacitor and diode clamped. The cascaded MLI uses series connected H-Bridge inverters, separate capacitors or DC sources, and less number of used components in each level[3-4]. The x level cascaded MLI uses (2x – 2) semiconductor switches and ((x – 1)/2) capacitors[3-4]. Flying capacitor topology uses capacitors to divide input DC voltages. The x level flying capacitor MLI uses (2x – 2) semiconductor switches and (x – 1) capacitors [3-4]. Diode clamped topology uses clamping diodes to limit voltage stress of semiconductor devices. The s level diode-clamped MLI uses (2x – 2) semiconductor switches, (x – 1) voltage sources, and (x – 1)(x – 2) diodes [5-6]. The separated DC sources multilevel inverter topology [7-9] has simple controls to convert renewable energy source to the grid.

A single phase inverter topologies suitable for PV application are presented in [l0-12].The single phase inverter topologies require an isolated DC supply so it is suitable to PV application and grid tie inverter [13-14]. The modular topologies with fewer semiconductor components and lower total harmonic distortion are becoming the interest of researchers in the last decades [11-12], and [15].

In this paper proposed a nine-level MLI based on two stages converter. The first one is high level frequency generator implemented by four buck DC-DC converters and the other one is H-bride inverter for polarity generator. The proposed multilevel inverter topology uses eight active switches and four passive switches where the diode-clamped, flying capacitor, and cascaded H-Bridge MLI needs 16 semiconductor switches and several capacitors or diodes. The proposed topology uses simpler switches configuration complexity and decreased number of used power switches. Second part of the paper describes about operation modes of single phase nine-level inverter and proposed pulse width modulation strategy. The third part describes about computational simulation, prototype results and the last part of shows the conclusion of the proposed topology.

II. RESEARCH METHOD

The proposed MLI requires eight active switches, four passive switches and 4 separated DC voltage sources (E) as shown at Fig. 1. The 4 buck DC-DC converters require four active switches and four passive switches and four DC voltage sources. This converter operates at high frequency. The H-Bridge inverter requires four active switches. This converter operates in the 50 Hz frequency.

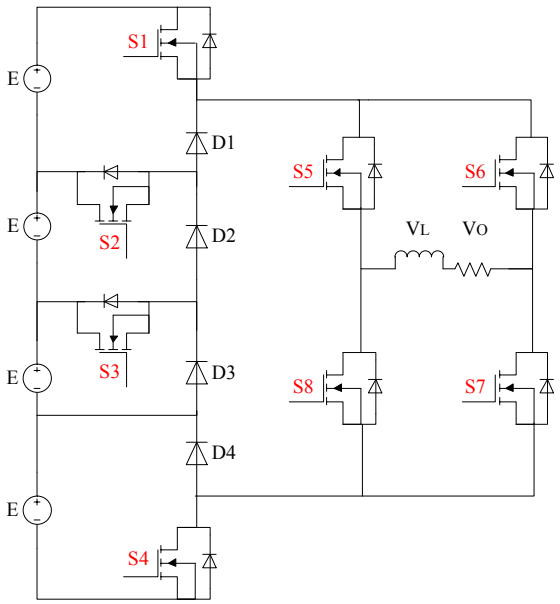


Fig. 1. The proposed nine-level inverter

The proposed nine-level inverter has two cycles: positive and negative. Fig. 2 - 6 is shown the modes of operation for a nine-level inverter on a half of positive output**.**

1. Mode of operation 1: maximum output voltage +4E: S1, S5, S7, and S4 are ON. All of the other switches are OFF. Fig. 2 shows the current flow in this mode. The equation for mode of operation 1 is given by:

$$V_{IN} = V_L + V_O$$

$$4E = L\frac{di_4}{dt} + V_O \quad (1)$$

$$L\Delta i_4 = (4E - V_O)t_{ON}$$

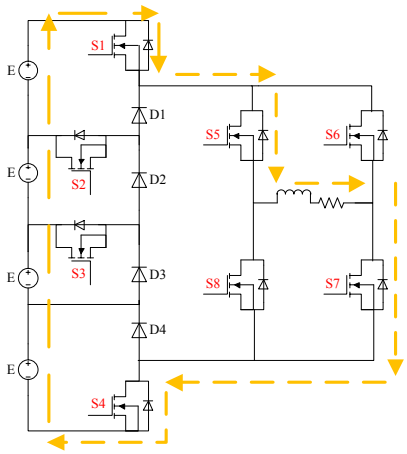


Fig. 2. Mode operation 1

2. Mode of operation 2: maximum output voltage +3E: S2, S5, S7, D1, and S4 are ON. All of the other switches are OFF. Fig. 3 shows the current flow in this mode and the equation for mode of operation 2 is given by:

$$V_{IN} = V_L + V_O$$

$$3E = L\frac{di_3}{dt} + V_O \quad (2)$$

$$L\Delta i_3 = (3E - V_O)t_{ON}$$

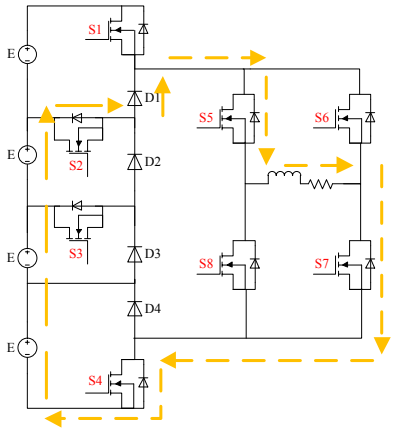


Fig. 3. Mode operation 2

3. Mode of operation 3: maximum output voltage +2E: S3, S5, S7, D1, D2 and S4 are ON. All of the other switches are OFF. Fig. 4 shows the current flow in this mode and the equation for mode of operation 3 is given by:

$$V_{IN} = V_L + V_O$$

$$2E = L\frac{di_2}{dt} + V_O \quad (3)$$

$$L\Delta i_2 = (2E - V_O)t_{ON}$$

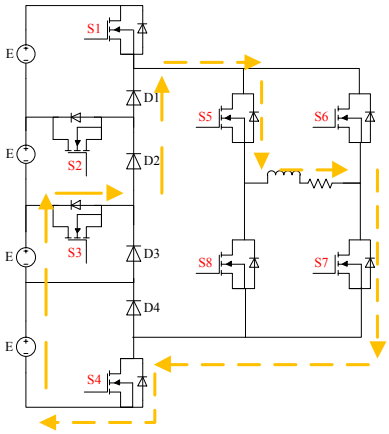


Fig. 4. Mode operation 3

4. Mode of operation 4: maximum output voltage +E: S5, S7, D1, D2, D3 and S4 are ON. All of the other switches are OFF. Fig. 5 shows the current flow in this mode and the equation for mode of operation 4 is given by:

$$V_{IN} = V_L + V_O$$

$$E = L\frac{di}{dt} + V_O \quad (4)$$

$$L\Delta i = (E - V_O)t_{ON}$$

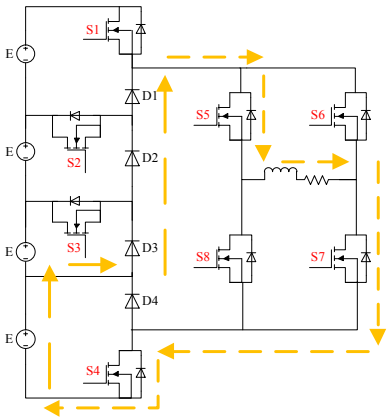
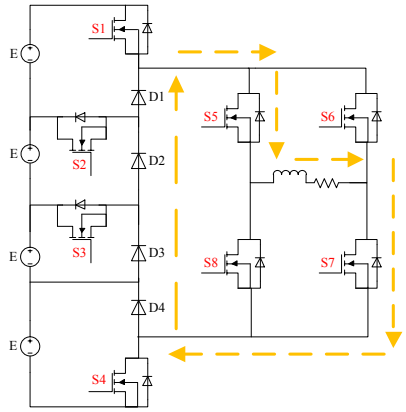


Fig. 5. Mode operation 4

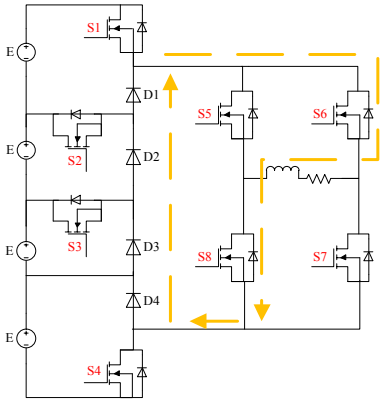
5. Mode of operation 5 and 6, zero output: this mode can be obtained with two switching combinations: D1, D2, D3, D4, 5, S7 are ON or D1, D2, D3, D4, S6, S8 are ON and all of the other switches are OFF. Terminal output is a short circuit and the voltage applied to the load terminals is zero. Fig. 6(a) and Fig. 6(b) show the current flow in this mode and the equation for mode of operation 5 and 6 are given by:

$$Vo = L\frac{di0}{dt} \quad (5)$$

$$L\Delta i0 = [Vo]tOFF$$



(a)



(b)

Fig. 6. Mode of operation 5 and 6. (a) Mode of operation 5, (b) Mode of operation 6

6. The mode of operation for a negative half- cycle can be achieved with mode of operation 1-4 however the switches operated in H-Bridge inverter are S6 and S8 while S5 and S7 are OFF.

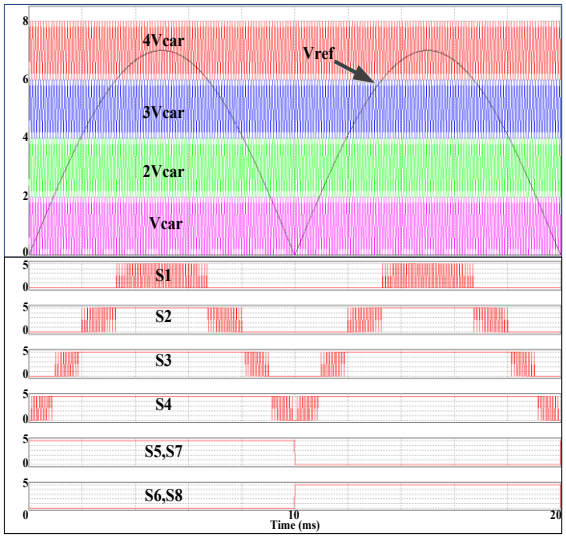


Fig. 7. The proposed sinusoidal pulse width modulation

Then modulated in Fig. 7 can be derived as follows:

$$Vo = \frac{Vref}{Vcar} \times E \quad (6)$$

This equation applies for operation mode 4 and 5

$$Vo = \frac{Vref}{2Vcar} \times E \quad (7)$$

This equation applies for operation mode 3 and 5

$$Vo = \frac{Vref}{3Vcar} \times E \quad (8)$$

This equation applies for operation mode 2 and 5

$$Vo = \frac{Vref}{4Vcar} \times E \quad (9)$$

This equation applies for operation mode 1 and 5

Where:

V_o : Modulation output waveform

V_{ref} : Signal Reference

V_{car} : Signal Carrier

By this condition, MLI could be operated as nine-level inverter (the eq.6 – 9), seven-level (the eq.7 – 9), five-level (the eq.8 – 9), and three-level (the eq.9)

Fig. 8 shows the proposed flowchart diagram for MLI. The generating reference signal and carrier signal by look-up table data that had been simulated using Power simulator software. After the generating a reference signal and carrier signal will be compared to choose which switches are ON.The sinusoidal pulse width modulation controller is generated by PIC18F4550 micro-controller. The prototype of proposed MLI was made using IRFP250N MOSFET and was gated using TLP250 gate driver circuitry shown in Fig. 9.

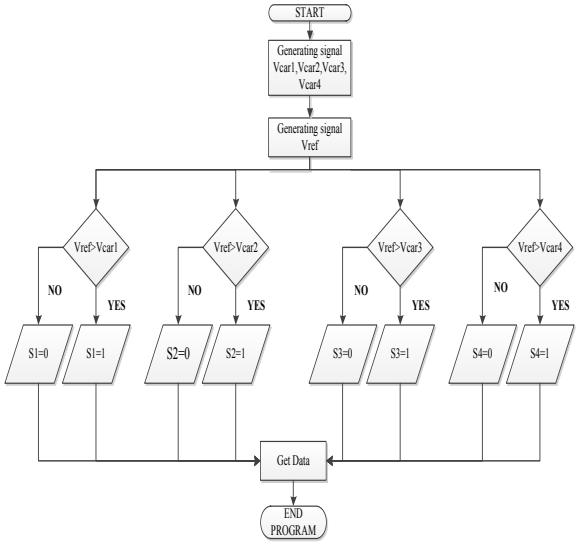


Fig. 8. The proposed flowchart diagram

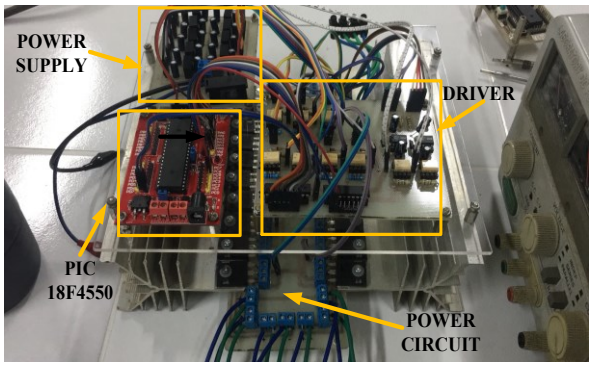


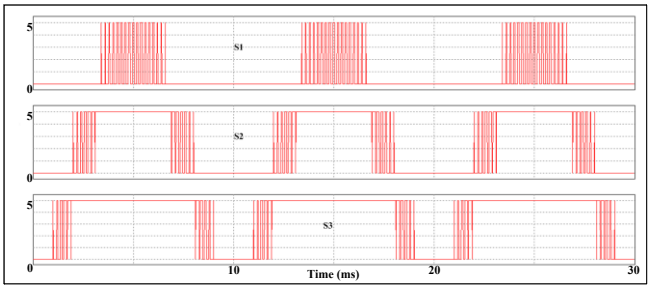
Fig. 9. Prototype of the proposed topology

III. Results and Analysis

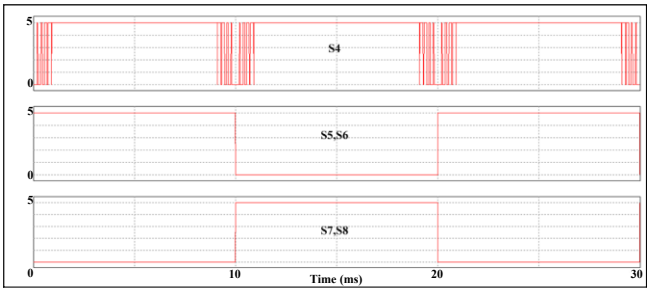
The single-phase nine-level inverter is simulated in Power simulator software implemented in the laboratory based on parameter on Table 1. The gate pulse for high frequency switches and low frequency switches generated simulation is shown in Fig. 10.

Table. I Parameter of Simulation and Prototype Implementation

Parameters		Unit
Vin	:	48 Volt DC
Inductor	:	5mH
Resistive Load	:	45 Ohm
Switching Frequency	:	5KHz , 50 Hz



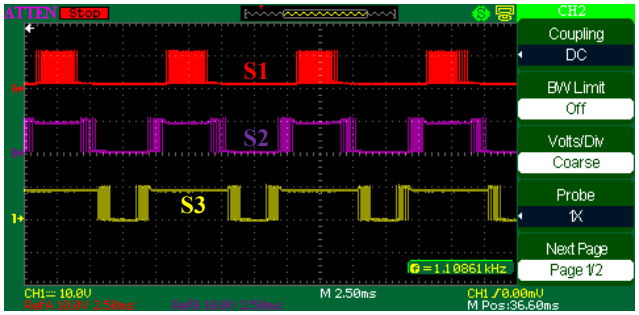
(a)



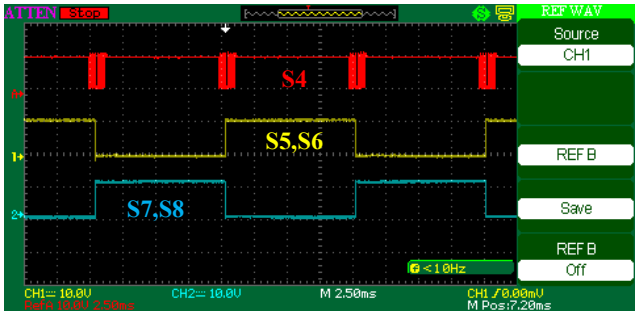
(b)

Fig. 10. Simulated waveform : (a) Switching on S_1– S_3
(b) Switching on S_4– S_8

Fig. 10(a) and Fig. 11(a) show the sinusoidal pulse width modulation used for S1– S3. Fig. 10(b) and Fig. 11(b) show the sinusoidal pulse width modulation used in S4 and the active switch S5 – S8 are reversing polarity pulse at 50 Hz. The prototype of proposed topology uses 4 x 12 volt separated DC voltage sources to generate nine-level voltage at maximum of 48 volts.



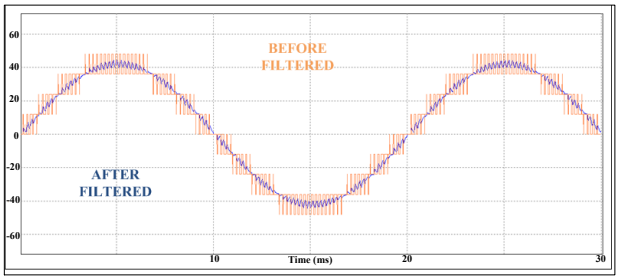
(a)



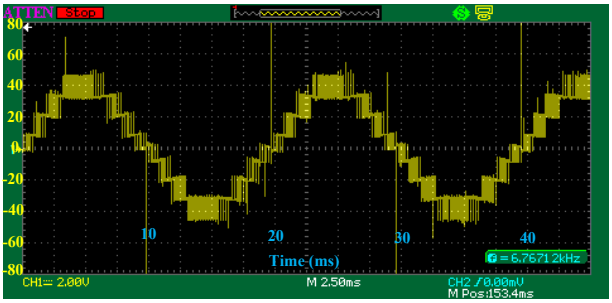
(b)

Fig. 11. Implemented waveform : (a) Switching on S_1– S_3
(b) Switching on S_4-S_8

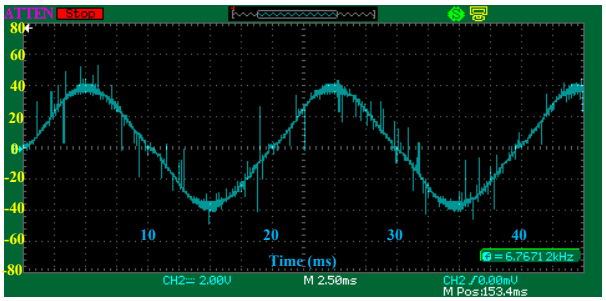
Fig. 12(a) shows the computational simulation result of nine-level MLI output waveform. Fig. 12(b) shows the experimental result of nine-level MLI output waveform. The voltage levels prototype of proposed topology are +48V, +36, +24V, +12V, 0, -12V, -24V, -36 and -48V. The inductor filter used to obtain fundamental voltage. Fig. 13(a) shows the output voltage and current waveform from simulation. The experiment on laboratory tested is shown on Fig. 13(b).



(a)

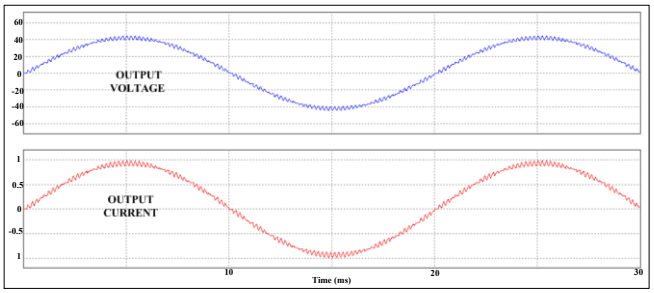


(b)

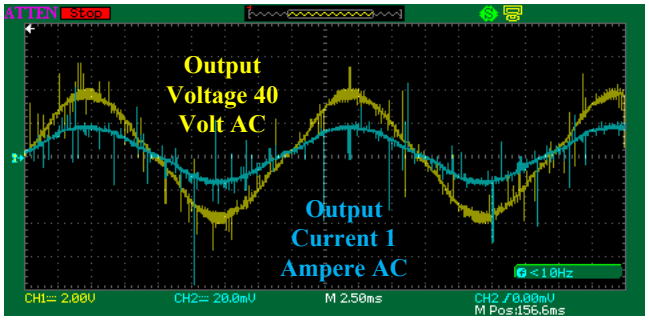


(c)

Fig. 12. Inverter voltage output: (a) Simulation before filtered and after filtered (b) Laboratory experiment before filtered (c) Laboratory experiment after filtered



(a)



(b)

Fig. 13. Inverter voltage and current output : (a) Simulation (b) Laboratory experiment

IV. Conclusions

The nine-level inverter topology in this paper consists of level generator and polarity generator. The level generator used high frequency switching and polarity generator used low frequency switching. The sinusoidal pulse width modulation for proposed topology has lesser difficulties since only positive carriers are generated for SPWM control. The prototype results of the proposed topology for a nine-level inverter are validated in this paper. The results show that the proposed topology can be used as a nine-level inverter with a simple SPWM effectively.

References

[1] Carlo Cecati, Fabrizio Ciancetta, and Pierluigi Siano, "A Multilevel Inverter for Photovoltaic Systems With Fuzzy Logic Control", IEEE Transactions On Industrial Electronics, Vol. 57, No. 12, December 2010.

[2] Sérgio Daher, Jürgen Schmid, and Fernando L. M. Antunes, "Multilevel Inverter Topologies for Stand-Alone PV Systems", IEEE Transactions On Industrial Electronics, Vol. 55, No. 7, July 2008.

[3] R. Stala, S. Pirog, et all, "Results of investigation of multicell converters with balancing circuit—Part I," IEEE Trans. Ind. Electron., vol. 56, no. 7, p. 2610–2619, Jul. 2009.

[4] P. Lezana and J. Rodriguez, "Mixed multicell cascaded multilevel inverter," in Proc. IEEE ISIE, 2007, pp. 509–514.

[5] M. M. Renge and H. M. Suryawanshi, "Five-level diode clamped inverter to eliminate common mode voltage and reduce dv/dt in medium voltage rating induction motor drives," IEEE Trans. Power Electron., vol. 23, no. 4, pp. 1598–1160, Jul. 2008

[6] Mario Marchesoni and Pierluigi Tenca, "Diode-Clamped Multilevel Converters: A Practicable Way to Balance DC-Link Voltages", IEEE Transactions On Industrial Electronics, Vol. 49, No. 4, August 2002.

[7] S. G. Song, F. S. Kang, and S.-J. Park, "Cascaded multilevel inverter employing three-phase transformers and single dc input," IEEE Trans. Ind. Electron., vol. 56, no. 6, pp. 2005–2014, Jun. 2009.

[8] Sreedhar Madichetty, Abhijit Dasgupta, "Modular Multilevel Converters Part-I: A Review on Topologies, Modulation, Modeling and Control Schemes", International Journal of Power Electronics and Drive System (IJPEDS), Vol. 4, No. 1, March 2014 pp. 36~50.

[9] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Pe´rez, "A survey on cascaded multilevel inverters," IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2197–2206, Jul. 2010.

[10] V.G. Agelidis, D.M. Baker, W.B. Lawrance, C. V. Nayar, "A Multilevel PWM Inverter Topology for Photovoltaic Application," IEEE Trans. Ind. Electron., on, vol. II, pp. 589-594. 1997

[11] Leonardus Heru Pratomo, F. Danang Wijaya, and Eka Firmansyah, "A Simple Strategy of Controlling a Balanced Voltage Capacitor in Single Phase Five-Level Inverter", International Journal of Power Electronics and Drive System (IJPEDS), Vol. 6, No. 1, March 2015, pp. 160~167.

[12] E. Najafi, and A. H. M. Yatim, "Design and Implementation of a New Multilevel Inverter Topology, vol. 59, no. 11, pp. 4148-4154, Nov. 2012.

[13] Leonardus Heru Pratomo, F. Danang Wijaya, and Eka Firmansyah," Impedance Matching Method in Two-Stage Converters for Single Phase PV-Grid System', International Journal of Electrical and Computer Engineering (IJECE), Vol. 5, No. 4, August 2015, pp. 626~635

[14] N. A. Rahim, K. Chaniago, and J. Selvaraj, "Single-Phase Seven-Grid-Connected Inverter for Photovoltaic System," IEEE Trans. Ind. Electron., vol. 58, no. 6, pp. 2435-2443, Jun. 2011.

[15] J. Rodriguez, J. S Lai, and F. Z. Peng "Multilevel inverters: a survey of topologies, controls, and applications" IEEE Trans. Ind. Electron, 2002,49(4), pp. 724-738

CERTIFICATE

This is to certify that

Natanael Novalutfi Prasetiyo

has contributed as

Presenter

in The 5th International Conference on Information Technology, Computer and Electrical Engineering (ICITACEE) 2018
in Semarang Indonesia, September, 26-28th 2018

Ir M. Agung Wibowo, MM, MSc, PhD.
Dean of Faculty of Engineering Diponegoro University

Aghus Sofwan, ST, MT, PhD.
General Chair ICITACEE 2018