A Single Phase 11-Level Inverter for Photovoltaic Application

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Abstract—This paper presents a single phase 11-level inverter based on five buck DC-DC converters and H-bridge inverter topology with simple pulse width modulation method. The proposed inverter topology works in two operation steps; the first one for generating level and the second one for generating polarity. The pulse width modulation is employed to generate gating signals for power switches. The Separate DC sources can be replaced by renewable energy source. The complete system is simulated using Power Simulator Software for simulation results and micro-controller is used to generate gating signals, hardware results are presented to check the performance of the inverter in laboratory

Keywords—11-level inverter, Buck DC-DC converter, and H-bridge inverter.

I. INTRODUCTION

Clean energy receives attention as electricity source supplied by solar, wind, hydro, and other renewable energy source [1]. Photovoltaic (PV) source is used to fulfill the need of renewable energy resources along with the advantages of being maintenance and zero pollution [2]. In special case; the demand of PV electricity sources has grown 20%-25% per annum due to the decreasing costs and prices [2].

Electrical energy produced by PV is Direct Current. This system is incompatible with most standard electrical equipments supplied (Alternating Current). By this condition, they need an inverter to convert the Direct Current to Alternating Current [3]. The application of inverter needs voltage and current waveform with low Total Harmonic Distortion (THD) [4]. The conversion process could be done by conventional H-Bridge inverter [5]. However, the H-Bridge inverter is recommended for less sensitive equipment due to its quite high THD waveform, smaller output voltage level, poor electromagnetic stability, and high losses in switching [6].

In order to overcome the disadvantages of H-Bridge inverter, multilevel inverter (MLI) has been used. When the conventional H-Bridge inverter generates two level AC voltage from a DC source, multilevel inverter using multiple DC sources added together to generate smoother output voltage waveform. This inverter is capable to fulfill the demand of power quality and higher power rating along with lower THD_V or THD_I value [7]-[9]. The main classification of MLI is known as: cascaded H-Bridge [10]; diode-clamped [11]; and flying-capacitor [12]. The cascaded MLI uses series connected H-Bridge inverters, separate capacitors or DC sources, and less number of used components in each level[10]. The n level cascaded MLI uses (2n – 2) semiconductor switches and ((n – 1)/2) capacitors[10]. Diode-clamped MLI uses clamping diodes to limit voltage stress of semiconductor devices[11]. The n level diode-clamped MLI uses (2n – 2) semiconductor switches, (n – 1) voltage sources, and (n – 1)(n – 2) diodes[11]. Flying capacitor uses capacitors to divide input DC voltages. The n level flying capacitor MLI uses (2n–2) semiconductor switches and (n – 1) capacitors[12]. Despite the disadvantages of H-Bridge inverter has been overcome, these inverters has disadvantages such as: more semiconductor switches and diodes to use increasing the difficulty of controlling each switch [13],[14].

The proposed multilevel inverter topology uses 9 active switches and 5 passive switches where the diode-clamped, flying capacitor, and cascaded H-Bridge MLI needs 20 semiconductor switches and several capacitors or diodes. This topology proposes simpler switches configuration and decreased number of used semiconductor switches. Second part of the paper describes about operation modes of the proposed topology and proposed pulse width modulation strategy. The third part describes about computational simulation, prototype results and the last part shows the conclusion of the proposed topology.

II. RESEARCH METHOD

The proposed 11-level inverter uses 9 active switches (MOSFET), 5 passive switches (DIODE), and 5 separated DC voltage sources, Fig. 1. This topology has two operation parts. The first part is 5-buck DC-DC converters to generate voltage levels and the second part is H-Bridge inverter to generate polarity of the voltage level. The 5 buck DC-DC converters operate at high frequency switching to generate 5 positive voltage levels and the H-Bridge inverter operating at low frequency (50 Hz) to generate the polarity output.

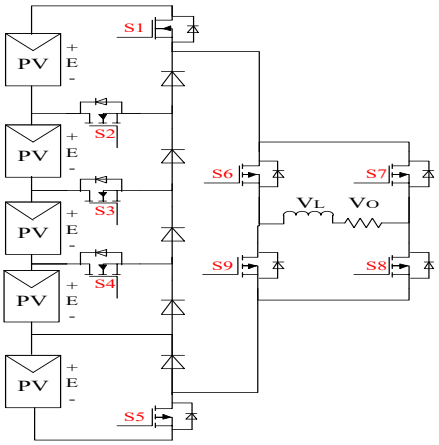


Fig. 1. The proposed 11-level multilevel inverter topology

The proposed nine-level inverter has two cycles: positive and negative. It would be explained the working principle of the proposed topology on a half of positive output:

1. Mode of operation 1: maximum positive output (+5E): The S1, S5, S6, and S8 are ON. All of the other switches are OFF. The equation for mode operation 1 is expressed as:

$$V_{IN} = V_L + V_O$$
$$5E = L\frac{di_5}{dt} + V_O \quad (1)$$
$$L\Delta i_5 = (5E - V_O)t_{ON}$$

2. Mode of operation 2: maximum positive output (+4E): The S2, D1, S5, S6, and S8 are ON. All of the other switches are OFF. The equation for mode operation 2 is expressed as:

$$V_{IN} = V_L + V_O$$
$$4E = L\frac{di_4}{dt} + V_O \quad (2)$$
$$L\Delta i_4 = (4E - V_O)t_{ON}$$

3. Mode of operation 3: maximum positive output (+3E): The S3, D2, D1, S5, S6, and S8 are ON. All of the other switches are OFF. The equation for mode operation 3 is expressed as:

$$V_{IN} = V_L + V_O$$
$$3E = L\frac{di_3}{dt} + V_O \quad (3)$$
$$L\Delta i_3 = (3E - V_O)t_{ON}$$

4. Mode of operation 4: maximum positive output (+2E): The S4, D3, D2, D1 S5, S6, and S8 are ON. All of the other switches are OFF. The equation for mode operation 4 is expressed as:

$$V_{IN} = V_L + V_O$$
$$2E = L\frac{di_2}{dt} + V_O \quad (4)$$
$$L\Delta i_2 = (2E - V_O)t_{ON}$$

5. Mode of operation 5: maximum positive output (+E): The D4, D3, D2, D1, S5, S6, and S8 are ON. All of the other switches are OFF. The equation for mode operation 5 is expressed as:

$$V_{IN} = V_L + V_O$$
$$E = L\frac{di_1}{dt} + V_O \quad (5)$$
$$L\Delta i_1 = (E - V_O)t_{ON}$$

6. Mode of operation 6 and 7: The zero output, this condition can be met with two switching possibilities: D1, D2, D3, D4, D5, S6, and S8 are ON or the D1, D2, D3, D4, D5, S7, and S9 are ON and all of the other switches are OFF. Terminal output is a short circuit condition and the voltage applied to the load terminals is zero. The equation for mode operation 6 and 7 are expressed as:

$$V_O = L\frac{di_0}{dt} \quad (6)$$
$$L\Delta i_0 = [V_O]t_{OFF}$$

7. The mode of operation 8 – 12 are a half negative output as the same as mode of operation 1-5

Based on mode of operation above can be created switching function table as in Table 1:

TABLE I. SWITCHING MODE OF OPERATION

Operation	S1	S2	S3	S4	S5	S6	S7	S8	S9	Vout
1	1	0	0	0	1	1	0	1	0	**5E**
2	0	1	0	0	1	1	0	1	0	**4E**
3	0	0	1	0	1	1	0	1	0	**3E**
4	0	0	0	1	1	1	0	1	0	**2E**
5	0	0	0	0	1	1	0	1	0	**E**
6	0	0	0	0	0	1	0	1	0	**0**
7	0	0	0	0	0	0	1	0	1	**0**
8	0	0	0	0	1	0	1	0	1	**-E**
9	0	0	0	1	1	0	1	0	1	**-2E**
10	0	0	1	0	1	0	1	0	1	**-3E**
11	0	1	0	0	1	0	1	0	1	**-4E**
12	1	0	0	0	1	0	1	0	1	**-5E**

Where:

1: switch is conducting.

0: switch is not conducting.

Thus, the overall operation mode (1) – (7) on a half of positive output, the inverter could be presented in matrix as follows:

$$\begin{bmatrix} V_O \\ V_O \\ V_O \\ V_O \\ V_O \\ V_O \end{bmatrix} = \begin{bmatrix} D_1 \\ D_2 \\ D_3 \\ D_4 \\ D_5 \\ D_6 \end{bmatrix} \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} 5E \\ 4E \\ 3E \\ 2E \\ E \\ 0 \end{bmatrix} \quad (7)$$

Where:

D1 = modulation index 1

D2 = modulation index 2

D3 = modulation index 3

D4 = modulation index 4

D5 = modulation index 5

D6 = modulation index 6

and

$$D = \frac{V_{ref}}{V_{car}} \quad (8)$$

The gating pulses of the inverter can be regulated by the modulation waveform of reference voltage (Vref) and carrier voltage (Vcar) to make sinusoidal pulse width modulation, Fig. 2.

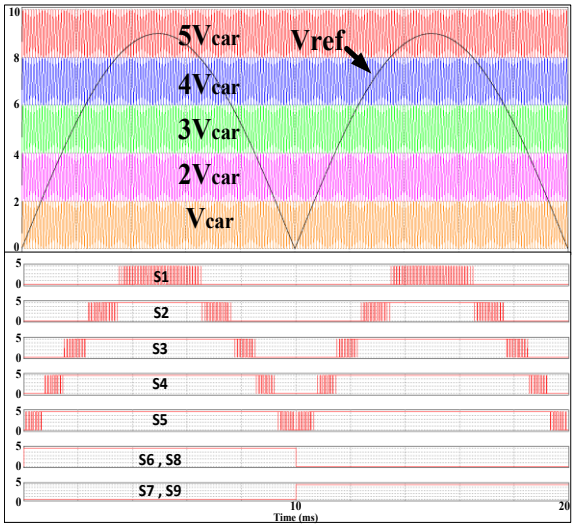


Fig. 2. Modulation of V_{ref} dan V_{car}

The value of the output voltage according to modulation signal can be presented as follows:

$$Vo = \frac{Vref}{Vcar} \times E \qquad (9)$$

This equation applies for mode operation (5) and (6)

$$Vo = \frac{Vref}{2Vcar} \times E \qquad (10)$$

This equation applies for mode operation (4) and (6)

$$Vo = \frac{Vref}{3Vcar} \times E \qquad (11)$$

This equation applies for mode operation (3) and (6)

$$Vo = \frac{Vref}{4Vcar} \times E \qquad (12)$$

This equation applies for mode operation (2) and (6)

$$Vo = \frac{Vref}{5Vcar} \times E \qquad (13)$$

This equation applies for mode operation (1) and (6)

Based on Table I; the proposed Sinusoidal Pulse Width Modulation (SPWM) scheme of 11-level MLI is seen in Fig. 3.

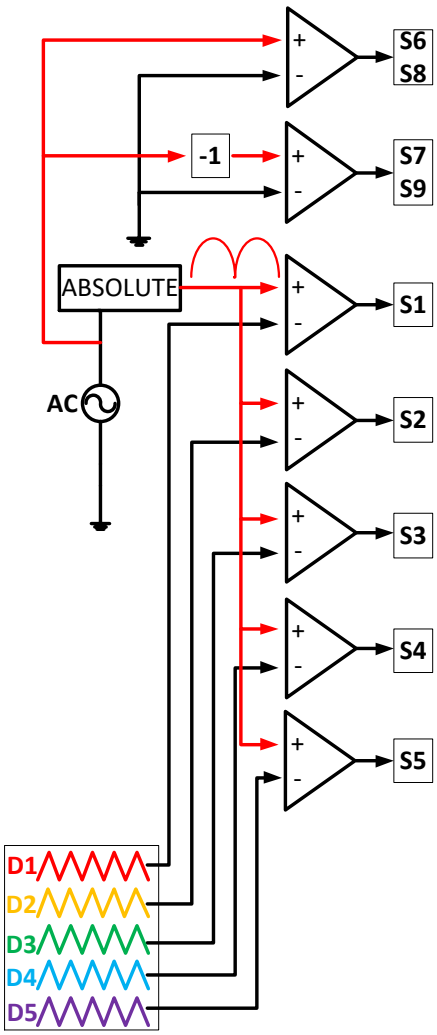


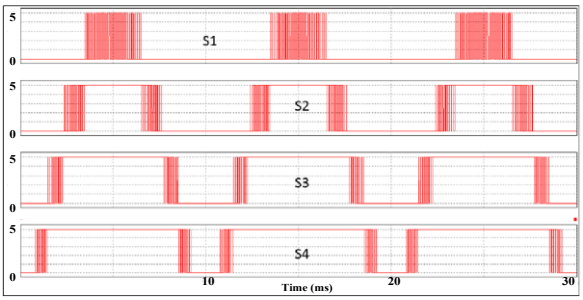
Fig. 3. Proposed SPWM technique

III. Results and Analysis

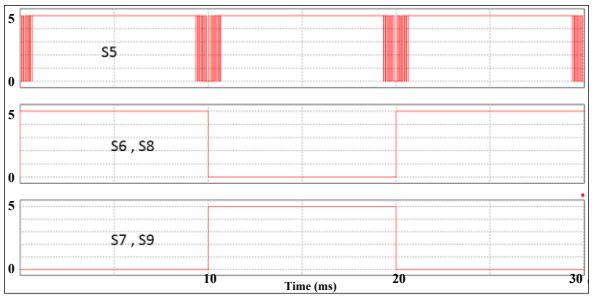
Verification of simulation and analysis had been conducted by laboratory testing through proposed topology prototype. The parameters used in laboratory testing would be shown in Table II. Control schematic (Fig. 2) was implemented with micro-controller PIC18F4550 using lookup table's data. The simulation of the control scheme in Fig. 2 was done with Power Simulator Software. Simulation process produced switching function and inserted it into micro-controller. Fig. 3(a) and 3(b), Fig. 4(a) and 4(b) shown the SPWM results for switches S1-S9 in micro-controller. The proposed topology prototype uses 5 DC sources at 12 volts to generate 11 level voltage at maximum of 60 volts.

TABLE II. Parameter of Simulation and Prototype Implementation

Parameters		Units
Vin	:	5 x 12 Volts DC
Inductor	:	2.5mH
Resistive Load	:	45 Ohm
Switching Frequency	:	5KHz , 50 Hz

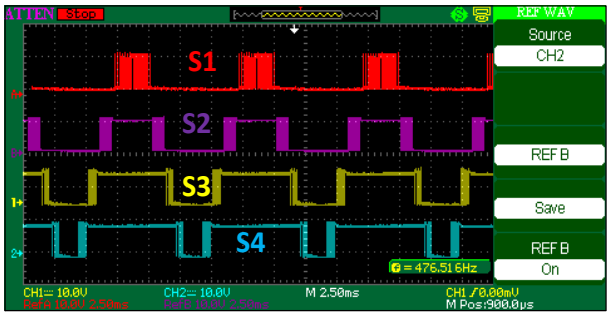


(a)

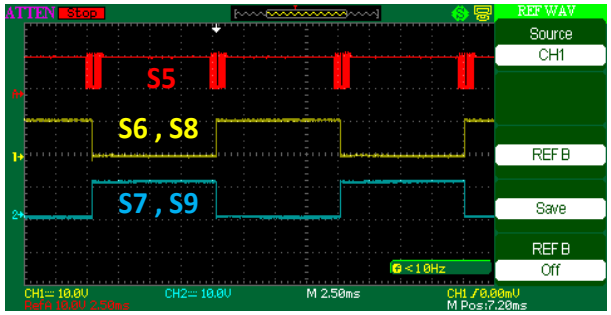


(b)

Fig. 4. Simulated waveform: (a) Switching on $S_1 - S_4$ (b) Switching on $S_5 - S_9$



(a)



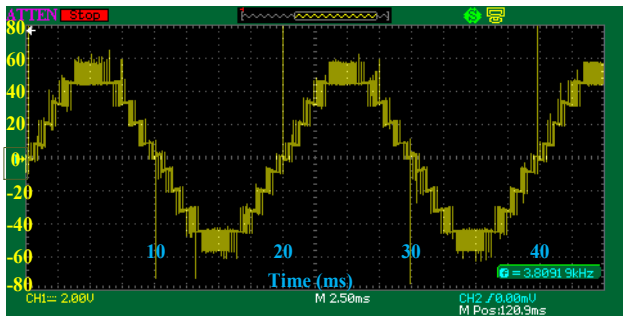
(b)

Fig. 5. Implemented waveform : (a) Switching on $S_1 - S_4$ (b) Switching on $S_5 - S_9$

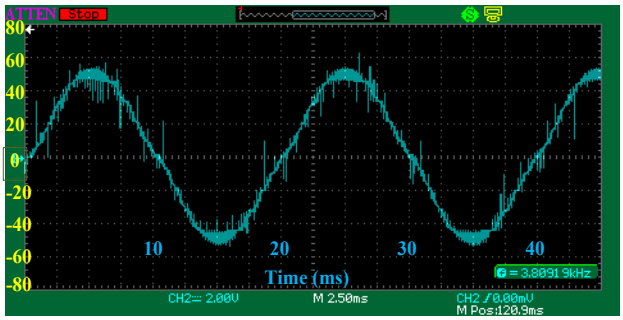
Fig. 4(a) and 5(a) show the SPWM used to S_1-S_4. Fig. 4(b) and 5(b) show SPWM used to S5 and polarity pulse inverter at 50 Hz used to S_6-S_9. This switching control scheme required power switch with high frequency switching for S_1-S_5 and power switch with low frequency switching for S_6-S_9. The 5 KHz carrier signal was modulated with 50 Hz sinusoidal signal to produce AC voltage with 50 Hz frequency.

Fig. 6 shows 11-level inverter output voltage from laboratory testing. The voltage level produced from level 1 to 11 are +60V, +48V, +36V, +24V, +12V, 0V, -12V, -24V, -36V, -48V, and -60V sequentially. The filter inductor can be used to obtain the fundamental voltage.

Fig. 7(a) shows the voltage and current output waveform through computer simulation and Fig. 7(b) shows the waveform of voltage and current output through laboratory testing.

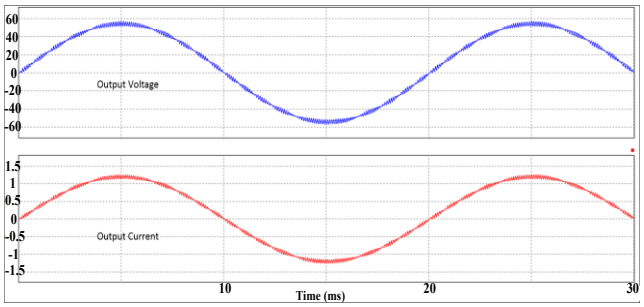


(a)

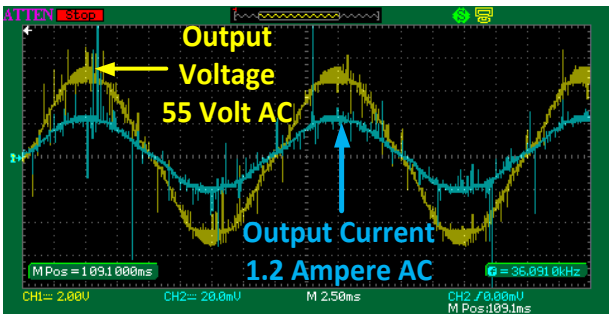


(b)

Fig. 6. Inverter voltage output (a)Before filtered (b) After filtered



(a)



(b)

Fig. 7. Inverter voltage and current output (a) Simulation (b) Laboratory testing

IV. CONCLUSIONS

This topology was presented in this paper consists of 5 level generator implemented by 5 buck DC-DC converters and polarity generator implemented by H-bridge inverter. So there is no need for controlling negative voltage instead the polarity reversing was done by H-Bridge inverter. The implemented 11-level inverter topology has more advantages compared to the conventional MLI; the proposed topology uses less semiconductor active switches. The high frequency switches can be operated at the fundamental frequency so overall cost and complexity of the circuit can be reduced. This topology is suitable for photovoltaic application. The computational simulation and prototype results confirm the validity of the proposed topology.

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CERTIFICATE

This is to certify that

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has contributed as

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