Design and Simulation of an Asymmetrical 11-Level Inverter for Photovoltaic Applications

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***Abstract*—Increasing demands of power conversion technology encourages multilevel converters emerge as a solution to overcome limitations at power ratings in conventional methods of power converters. This paper discusses about a new asymmetrical construction of an 11-level inverter, despite the focus on the following design, few comparisons of the conventional topological construction will be stated. Limitations in conventional types topologies often deals with its complexity and volume. It will be furthered mentioned how the asymmetrical topology of the 11-level inverter design deals and overcome these limitations and reduce harmonic distortions for grid-tied PV systems. The proposed construction is designed and simulated by PSIM software. Analysis of Real-Time Simulation of the proposed design results in a THD value of 1.19%**

***Index Terms*—Multilevel Inverter, Photovoltaic, SPWM, Alternative Energy**

I. Introduction

Power electronics are the core of modern application conversion systems. The increasing demands to improve efficiency, usage flexibility leads to technical challenges around the control method used and their topologies. Multilevel inverters could overcome the power ratings and handling limits by shared through ratings in the components of the switches. [1] These converter trends are largely applied to renewable technologies and industry appliances. [2] As the output of the PV cells are DC, and after maximizing the DC power output by the MPPT. DC power is converted to AC as a source for home and industrial appliances. [3], [4], [5]

Conventional construction of inverters are limited by their components power ratings. [6] As a result, methods of multilevel conversion is used to share and distribute power collective through the components. Most commonly known topologies are the flying-capacitor and diode-clamp constructions. But as levels are increased these builds up volume, cost and number of switches. Asymmetrical design generally satisfies this objective and with the increased levels, harmonic distortions which percentage nominals that are regulated by IEEE standards in output power are reduced. [3], [7]

Advantages of the construction increases demands of smaller, efficient, rigid types of multilevel inverters in time, resulting in reduced number of switches and maximizing their potential in distributed power. As these are the trends in modern usage power conversion multilevel inverter design. [8]

In response to the conventional limitations of inverters, this paper proposes a new asymmetrical 11-level inverter design, simulated with PSIM by PowerSimTech. As it will be covered later in Section II. that will discuss the proposed inverter circuit design and switching operations. Mentioned earlier, disadvantages of conventional methods of inverters (e.g two-stage converters) would deal mostly in relatively high harmonic values in output voltage. [9] Although in Section III. it will be stated the recommended practices for harmonic values by IEEE and could be considered how harmonic values in inverter design could be implemented in different types of applications. Even after implementing multilevel topologies (e.g diode clamp, flying capacitor, isolated power sources), the limits of the topology will cover around the number of switches used and switching operations that will affect effectiveness in further PV applications. [10], [11] The paper will also cover how the proposed 11-level inverter design would be capable to overcome conventional topology problems by the effective reduced number of switches to achieve a high number of n-levels and how this design could be useful to further research in higher n-level applications to reduce harmonic values even lower.

II. Inverter Design and Operations

A. Circuit Design Configuration

Design of the 11-Level Inverter is shown in Fig 1. The inverter is mainly divided into 2 stages; A(S1-S4) and B(S5-S8) which has a specific role in the proposed inverter operating principle. Stage A(S1-S4) is used to configure and construct the number of n-levels (11-level in proposed design) in the asymmetric inverter and Stage B(S5-S8) is used to change the

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polarity of the inverters Stage A(S1-S4) DC output resulting to a n-level AC output for grid-tied PV systems. [12]

Stage A(S1-S4) are directly connected to the DC power source, for this proposed 11-level inverter design, configuration of the DC source is divided to 3 isolated DC sources which nominal value is configured E, 2E, and 2E meaning the definition value in DC voltage of E are determined by the constructor while the switches series type, power ratings are still in high consideration. [12], [13]

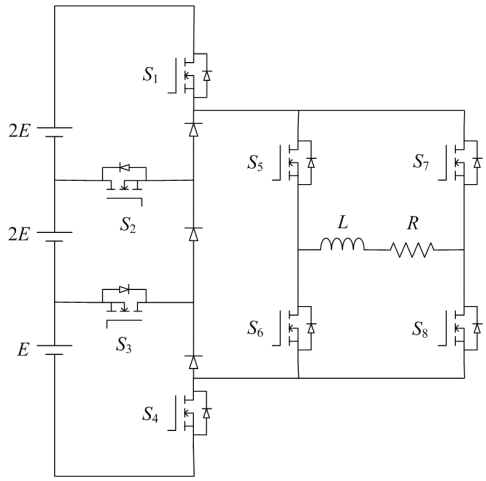


Fig. 1. Circuit Design

B. Switching Operation Modes

Switches configuration are operated in total of 11 mode levels, ranging from operation mode 0 - 10. The operation for mode 0 are achieved when all switches in Stage A(S1-S4) are conditioned OFF ”0” and Stage B(S5-S8), divided into 2 primary conditions; First condition achieved when switches paired S5, S8 conditioned ON ”1” while switches S6, S7 conditioned OFF ”0”. Second condition for mode 0 are when switches S6, S7 logically conditioned ON ”1” and switches S5, S8 conditioned OFF ”0”. Pairing switches in this operation are configured freewheeling (See Fig 2.).

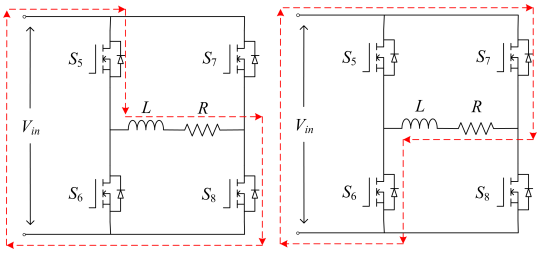


Fig. 2. Operation Mode 0

Where $V_{in} = 0$ as a result of switches Stage A(S1-S4) conditioned OFF ”0” and pairing switches in Stage B(S5-S8) (See Fig 1.) are conditioned ”1”. Therefore the result of this operation is analyzed before the inductive filter as $V_o = 0$.

Operation modes 1-5 (Seen in Fig 3-7.) are the basic constructing operations of the 11-Level inverter with stage B(S5-S8) operating switches S5 and S8.

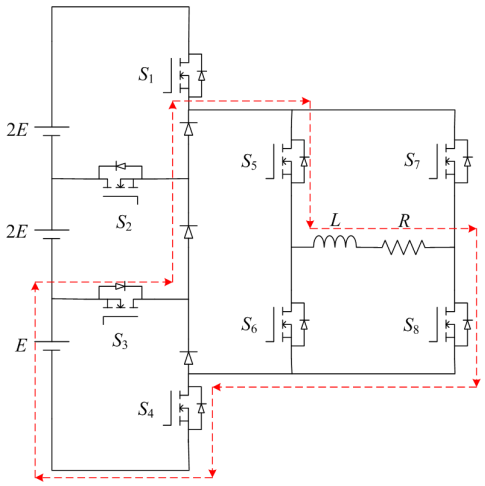


Fig. 3. Operation Mode 1

Seen in Fig 3. the operation for mode 1 are achieved when switches S3, S4 in Stage A(S1-S4) and S5, S8 in Stage B(S5-S8) closed.

Where $V_{in} = E$ as a result of switches S3, S4 in Stage A(S1-S4) and S5, S8 in Stage B(S5-S8) are conditioned ”1” or closed. Therefore the result of this operation is analyzed before the inductive filter as $V_o = E$.

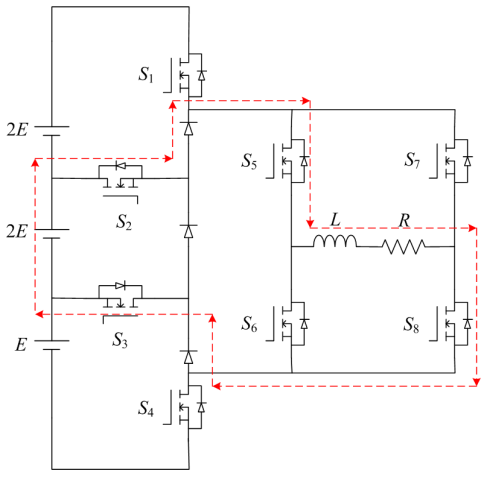


Fig. 4. Operation Mode 2

Fig 4. shows operation for mode 2, achieved when switches S2, S3 in Stage A(S1-S4) and S5, S8 in Stage B(S5-S8) closed.

Where $V_{in} = 2E$ as a result of switches S2, S3 in Stage A(S1-S4) and S5, S8 in Stage B(S5-S8) are conditioned ”1” or closed. Therefore the result of this operation is analyzed before the inductive filter as $V_o = 2E$.

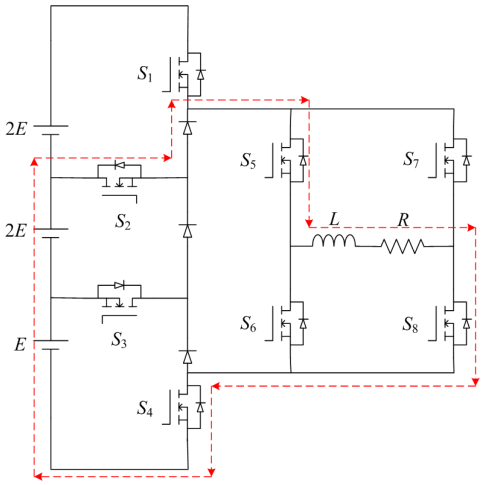


Fig. 5. Operation Mode 3

Described in Fig 5. operations mode 3 are achieved when switches S2, S4 in Stage A(S1-S4) and S5, S8 in Stage B(S5-S8) closed.

Where $V_{in} = E + 2E$ as a result of switches S2, S4 in Stage A(S1-S4) and S5, S8 in Stage B(S5-S8) are conditioned "1" or closed. Therefore the result of this operation is analyzed before the inductive filter as $V_o = 3E$.

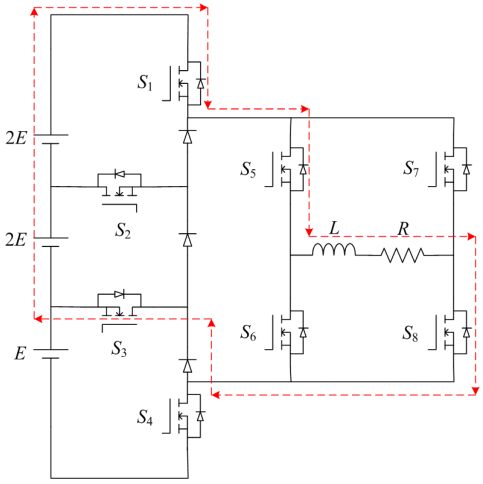


Fig. 6. Operation Mode 4

Fig 6. describes the operation for mode 4, achieved when switches S1, S3 in Stage A(S1-S4) and S5, S8 in Stage B(S5-S8) closed.

Where $V_{in} = 2E + 2E$ as a result of switches S1, S3 in Stage A(S1-S4) and S5, S8 in Stage B(S5-S8) are conditioned "1" or closed. Therefore the result of this operation is analyzed before the inductive filter as $V_o = 4E$.

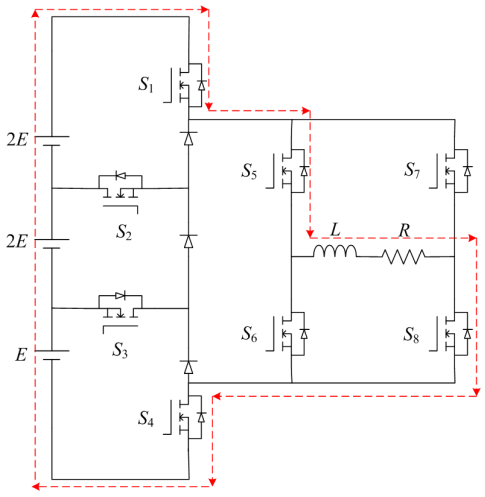


Fig. 7. Operation Mode 5

Shown in Fig 7., the operation for mode 5 are achieved when switches S1, S4 in Stage A(S1-S4) and S5, S8 in Stage B(S5-S8) closed.

Where $V_{in} = E + 2E + 2E$ as a result of switches S1, S4 in Stage A(S1-S4) and S5, S8 in Stage B(S5-S8) are conditioned "1" or closed. Therefore the result of this operation is analyzed before the inductive filter as $V_o = 5E$.

Operation modes 6-10 are the exact opposite polarity for modes 1-5. The half positive cycle of modes 1-5 are configured to oppose polarities by Stage B(S5-S8) switches S6, S7 configured "1" or ON resulting in a half negative cycle.

C. SPWM Gate Switching and Combinational Logic Circuit

Pulse-Width Modulation switching in stage A(S1-S4) gates are constructed by the absolute value of $\frac{1}{2}\lambda$ compared with 5 tiers of triangular waves A, B, C, D, E with different DC offsets (See Table 2. and Fig 8.) with carrier frequency of 10kHz (Described in Section III.). Table I. describes the configuration of overall switches to achieve the level desired.

TABLE I
SPWM GATE SWITCHING

Stage A				Stage B				Vo
S1	S2	S3	S4	S5	S6	S7	S8	
1	0	0	1	1	0	0	1	5E
1	0	1	0	1	0	0	1	4E
0	1	0	1	1	0	0	1	3E
0	1	1	0	1	0	0	1	2E
0	0	1	1	1	0	0	1	E
0	0	0	0	1	0	0	1	0
0	0	0	0	0	1	1	0	0
0	0	1	1	0	1	1	0	-E
0	1	1	0	0	1	1	0	-2E
0	1	0	1	0	1	1	0	-3E
1	0	1	0	0	1	1	0	-4E
1	0	0	1	0	1	1	0	-5E

As it is shown in Table I. the output voltage of inverter circuit will result in the same voltage as the input voltage (before passing through inductive filter).

In order to achieve the desirable gate switching, a combinational logic circuit is configured (See Fig 8.).

TABLE II
TRUTH TABLE IN STAGE A(S1-S4)

A	B	C	D	E	S1	S2	S3	S4
1	0	0	0	0	0	0	1	1
1	1	0	0	0	0	1	1	0
1	1	1	0	0	0	1	0	1
1	1	1	1	0	1	0	1	0
1	1	1	1	1	1	0	0	1

Table II. describes how we could derive the boolean expression by analyzing the logic circuits used in the design simulation. Resulting to the boolean algebra expression.

$$S_1 = D$$
$$S_2 = B \oplus D$$
$$S_3 = ((A \oplus C) \oplus D) \oplus E$$
$$S_4 = (((A \oplus B) \oplus C) \oplus D) \oplus E$$

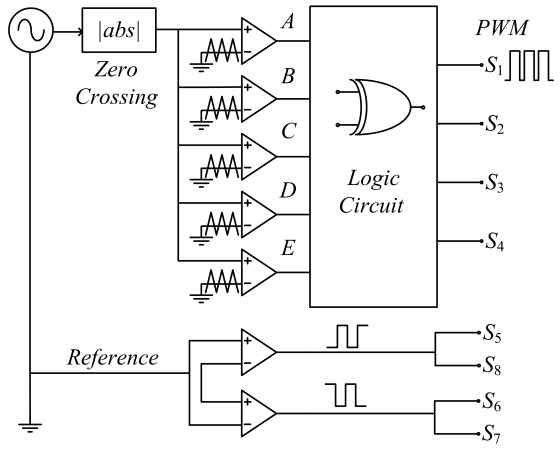


Fig. 8. Switching Configuration and Control Circuit

Fig 8. describes the overall control circuit for the proposed inverter. Shown by the boolean expression, the logic circuit diagram is consisted of XOR logic gates to achieve the desired truth table for the 11-level inverter. Input of the logic circuit consists of sinusoidal pulse width modulation (Discussed further in Section III.) achieved by comparing the half positive cycle of a reference sine wave and a triangular carrier waveform.

III. SIMULATION AND HARMONIC ANALYSIS

Real-time simulation design and analysis of the proposed design asymmetrical 11-level inverter are simulated in PSIM software by PowerSimTech. Fig 8. describes the design control circuit output sinusoidal pulse width modulation (SPWM) produced by the comparison of reference and carrier waves, further analysis of the output SPWM decoded by combinational logic circuits will be further discussed and seen in Fig 11. harmonic distortions of the output waveform of the proposed asymmetrical 11-level inverter design will be furthered described and analyzed in Fig 12. simulation parameters for the proposed inverter circuit are described in Table III.

TABLE III
SIMULATION PARAMETER

Device	Units
DC input E	1V
DC input 2E	2V
Inductive Filter	2mH
Load Resistor	12Ω
Reference AC Peak Amplitude	10V
Reference AC Frequency	50Hz
Carrier Triangular Vpp	2V
Carrier Triangular Frequency	9kHz
Carrier Duty Cycle	0.5
DC Offset Carrier A	0V
DC Offset Carrier B	2V
DC Offset Carrier C	4V
DC Offset Carrier D	6V
DC Offset Carrier E	8V
Print Time	0.02s

In order to achieve sinusoidal pulse width modulation (SPWM), sine wave reference are compared to five triangular carriers with different DC offset values (Described in Table III.) the offsets value and Vpp are configured to adjust the reference sine waveform half positive cycle with the frequency of each carriers 10kHz (Table III.). Fig 10. shows the sinusoidal pulse width modulation result for carrier waveforms A, B, C, D, E.

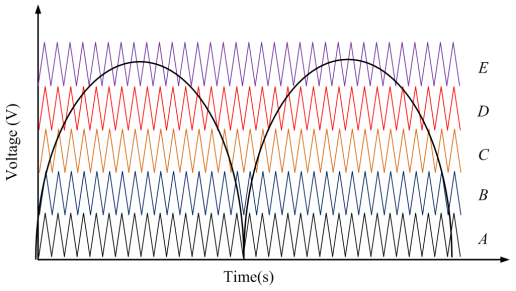
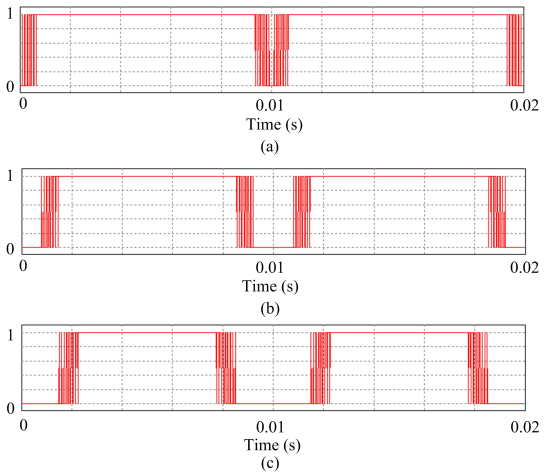


Fig. 9. Triangular Wave 10kHz Comparison with Absolute Value of $\frac{1}{2}\lambda$ Sine Wave 50Hz (Triangular Wave Frequency are not up to Scale)



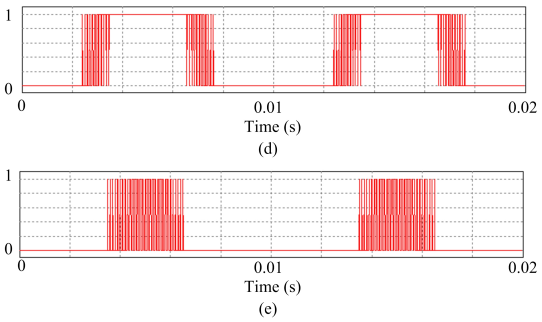


Fig. 10. SPWM A (a), SPWM B (b), SPWM C (c), SPWM D (d), SPWM E(e)

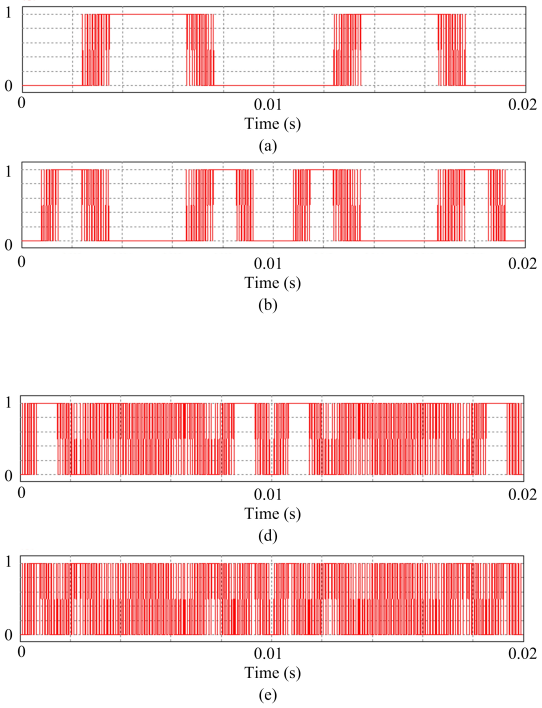
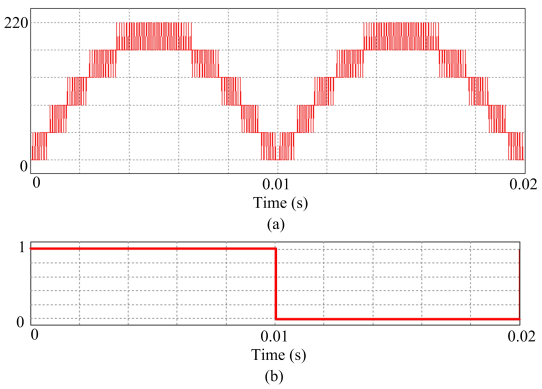


Fig. 11. SPWM Decoded by Logic Circuits for S1 (a) S2 (b) S3 (c) S4 (d)

Fig 9. shows the fundamental half wave SPWM to construct the 11-level output. Fig 10. input SPWM for switches at Stage A(S1-S4) are decoded through the combinational logic circuits in resulting to output shown in Fig 11. mentioned in switching configuration and control circuit Section II (See Fig 8.).



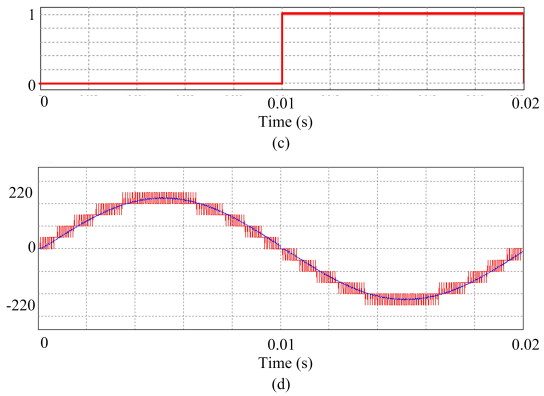


Fig. 12. Output for Switches Stage A(S1-S4) (a) Positive Zero Crossing Detection (b) Negative Zero Crossing Detection (c) 11-Level AC Output and Fundamental Voltage Analyzed at Load(d)

Fig 12.(a) shows the output for switches S1-S4. After the output SPWM analyzed (See Fig 10.), the polarization of the waveform is processed through Stage B(S5-S8) positive zero crossing detection (Fig 12.(b)) and negative zero crossing detection (Fig 12.(c)) resulting to an 11-level AC waveform.(Fig 12.(d)). Output is the filtered by an inductor described at Table 3.

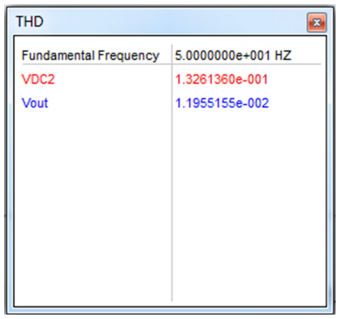


Fig. 13. THD Value Analyzed at 11-Level Output (VDC2) and Filtered by Inductor 2mH (Vout)

Seen on Fig 13. THD level analyzed at load with 50Hz output frequency. After installing inductive filter 2mH at load, the output voltage becomes smoother resembling more of an ideal 50Hz sine wave. THD value of proposed design is 1.19% (Vout)

IV. Conclusion

This paper has covered mainly in the proposed design for the asymmetrical 11-level inverter. Compared to the conventional multilevel inverter topology limitations (e.g. flying capacitor, diode clamp) which deals on inverter size and number of switches The asymmetrical 11- level inverter uses less number of gate switches for a higher number of n-levels. The proposed design focuses on grid-tied utility-scales PV systems application purposes. Adjustments for purpose satisfaction of the proposed design, the amount of component switches used and the flexibility of the design for the output levels produced are highly considered.

The proposed inverter construction is modified for PV implementations. Photovoltaic cells will produce

a certain DC power generator which values are maxed through the maximum power point tracker. DC input would be later used to power the inverter achieving in a multilevel AC output.

Mentioned in Section III., the THD value for this design analyzed and observed by Real-Time simulation PSIM software by PowerSimTech is 1.19% which is within range of IEEE standards 5% for harmonic voltage limits for power producers (public utilities or co-generators) at 2.3 - 69kV, 2.5% for 69 - 138 kV and 1.5% for $\geq$138kV.

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