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Hardware Implementation of an Asymmetrical 11-Level Inverter with Automatic Boost Charge Control in PV Applications

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***Abstract*—The increasing electricity demands for residential purposes results in the development of renewable photovoltaic standalone systems. With power converter technology as the core of the design; an undesirable harmonic distortion which affects the durability of electric equipment emerges from the construction that is above recommended practice standards. For decades, continuous research for the means to reduce harmonics in the power inverter unit of the system leads to multilevel technology. Nevertheless, the conventional topology of inverters would often deal with volume building and analysis complexity as the number of level increases. This paper discusses a further hardware implementation of the unique asymmetrical design of an 11-level inverter with an efficient number of reduced switches to achieve a higher level demand. This inverter is designed for single phase off-grid photovoltaic system application. The first verification of this research is a simulation design of the proposed topology. Finally, the hardware implementation which is done in a laboratory test environment, the THD_i test value is recorded 3.43% for the fundamental current of 4.72A at a frequency of 50Hz measured with the HIOKI 3286-20 power meter THD record function.**

***Index Terms*—Renewable Energy, Photovoltaic, Multilevel Inverter**

I. Introduction

The two fundamental aspects of power generation system expectations are an effective distribution reach of electricity and a stable supply system output [1]. With the increasing number of growing population and advancing technology over the year, the demands of a stable and even electricity distribution have never been more vital [2]. High usage of hydrocarbon deposits overtime gradually affects the biosphere. Furthermore, particularly in developing countries, the power generation main distributor often fails to meet the required demands of general usage, especially in residential purposes [3], [4]. Continuous research on renewable energy harvesting has been a vital point in the response of carbon emission issues combined with a high demand for an even electricity distribution throughout the area [5]. However, the variety of renewable sources are highly dependent on its geographical locations [6], as in the type of renewable energy accumulated at tropical regions quite differ from sub-tropical counterparts which could diverge from geothermal energy for volcanic locations, wind energy for temperate maritime climates and solar energy (photovoltaic) for high daylight distributed areas, [7] which will be covered specifically on the modification and development of the inverter unit topology and design [8].

Photovoltaic(PV) standalone system operations are constructed to provide electricity needs by the common household demands to compensate for the lack of energy distributed [9], [10]. The core concept of the system operations is as follows; photovoltaic cells generate DC electricity from converting photons from solar rays into a flow of electrons, the direct current generated is then extracted to a maximum value in the maximum power point tracker unit (MPPT) later used to charge the battery unit (optional if electricity required for later usage). From this point, DC power is converted to a stable AC power source with inverter technology [11], [12]. Basic designs of inverters (e.g. unipolar, bipolar inverters) unintentionally produce harmonic values which affect electric equipment (load) durability. Harmonic distortions itself is recommended below 5% for harmonic limits of power producers at 2.3 – 69.0 kV [13]. Means of reducing the harmonic contents of the converter unit encourage multilevel technology [14], which varies in commonly used topologies (e.g. diode-clamp, flying capacitor). But even with the common topology, increasing the level would result in a complex analysis and volume build which is considered inefficient [15], [16]. In response to the comparatively high harmonic distortion from the previous generation of inverter builds, a unique asymmetrical topology which in this case an asymmetrical 11-level inverter that uses less number of switches in the construction, purposed for single phase is verified by simulation [17].

This paper discusses and investigates a hardware implementation performance of the asymmetrical 11-level inverter in a single phase off grid application while excluding the microcontroller program algorithm. In Section 2, the principles of operation modes are analyzed to obtain a proposed model of the modulation strategy. The PV off grid system depends on a two stage process converter: As the first stage is a boost DC-DC

converter integrated with MPPT, while the other is the discussed asymmetrical 11-level voltage controlled inverter for residential applications. In Section 3, the verification of this strategy would be established by simulation and laboratory hardware tests. The hardware outcome itself is compared by IEEE standard for harmonics limits of power implementations (Below 5% for 2.3 - 69kV usage) [13] such in Indonesian PT. PLN (Persero) 220VAC/50Hz standard distribution usage as further in Section 4. the THD values would be fully analyzed and reported.

II. Research Method

A. Inverter Design

The proposed inverter design is shown in Fig 1. This asymmetrical construction is divided in a two step process; the first process is the level generation (S_1 – S_4) and the second part of the design is the polarirty generator (S_5 – S_8).

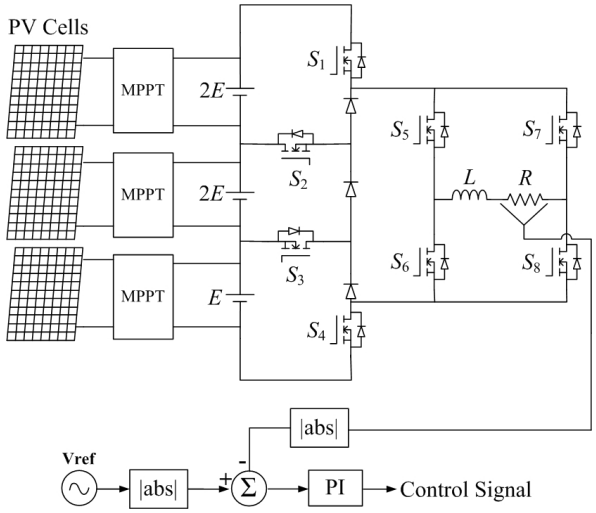


Fig. 1. Circuit Design of the Asymmetrical 11-Level Inverter [17]

The basic operation mode principles of the 11-level inverter are derived in operation modes 1-5 and the freewheeling modes;

1) Operation Mode 1:
When the power switches: S_3, and S_5 are conducted; the current from the VDC source(E) will flow to the load and return to the VDC source(E) through the S_8 and S_4 power switches. The equation for this operation is represented in Equation (1).

$$E = L\frac{di}{dt} + V_O \tag{1}$$

2) Operation Mode 2:
When the power switches: S_2, and S_5 are conducted; the current from the VDC source(2E) will flow to the load and return to the VDC source(2E) through the S_8 and S_3 power switches. The equation for this operation is represented in Equation (2).

$$2E = L\frac{di}{dt} + V_O \tag{2}$$

3) Operation Mode 3:
When the power switches: S_2, and S_5 are conducted; the current from the VDC source(3E) will flow to the load and return to the VDC source(3E) through the S_8 and S_4 power switches. The equation for this operation is represented in Equation (3).

$$(E + 2E) = L\frac{di}{dt} + V_O \tag{3}$$

4) Operation Mode 4:
When the power switches: S_1, and S_5 are conducted; the current from the VDC source(4E) will flow to the load and return to the VDC source(4E) through the S_8 and S_3 power switches. The equation for this operation is represented in Equation (4).

$$(2E + 2E) = L\frac{di}{dt} + V_O \tag{4}$$

5) Operation Mode 5:
When the power switches: S_1, and S_5 are conducted; the current from the VDC source(5E) will flow to the load and return to the VDC source(5E) through the S_8 and S_4 power switches. The equation for this operation is represented in Equation (5).

$$(E + 2E + 2E) = L\frac{di}{dt} + V_O \tag{5}$$

6) Freewheeling Modes:
When the power switches: S_5, and S_8 conducts, the current flow will be on a freewheeling state to the load for a positive value. While the combination of switches S_6, and S_7 results in a freewheeling state for a negative value. Both represented in Equation (6).

$$0 = L\frac{di}{dt} + V_O \tag{6}$$

Based on the operation modes (1 - 6), the polarity generator always operate in a 50 Hz frequency to produce a half positive cycle and a half negative cycle. The gate switching logic for operation modes are represented in Table 1. The relation between equations (1 - 6) could be expressed in a matrix function seen in Equation (7) in a steady-state operation at a positive value.

$$V_O = M \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} 5E \\ 4E \\ 3E \\ 2E \\ E \\ 0 \end{bmatrix} \tag{7}$$

Where M is defined as the index modulation

TABLE I
11-LEVEL OUTPUT GATE SWITCHING CONFIGURATION

Level Generator				Polarity Generator				Vo
S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	
1	0	0	1	1	0	0	1	5E
1	0	1	0	1	0	0	1	4E
0	1	0	1	1	0	0	1	3E
0	1	1	0	1	0	0	1	2E
0	0	1	1	1	0	0	1	E
0	0	0	0	1	0	0	1	0
0	0	0	0	0	1	1	0	0
0	0	1	1	0	1	1	0	-E
0	1	1	0	0	1	1	0	-2E
0	1	0	1	0	1	1	0	-3E
1	0	1	0	0	1	1	0	-4E
1	0	0	1	0	1	1	0	-5E

B. Logic Decoder

The process of constructing the unique sinusoidal pulse width modulation (SPWM) of the asymmetrical inverter by applying The truth logic of the decoder as a base to design for the boolean algebra decoding sequence as described below

$$S_1 = D$$
$$S_2 = B \oplus D$$
$$S_3 = ((A \oplus C) \oplus D) \oplus E$$
$$S_4 = (((A \oplus B) \oplus C) \oplus D) \oplus E$$
$$S_5 = S_8 = positive\ value$$
$$S_5 = S_8 = negative\ value$$

The expression for the level generator logic decoding sequence could be seen for each power switches. The control circuit for the 11-level inverter is shown in Fig 2.

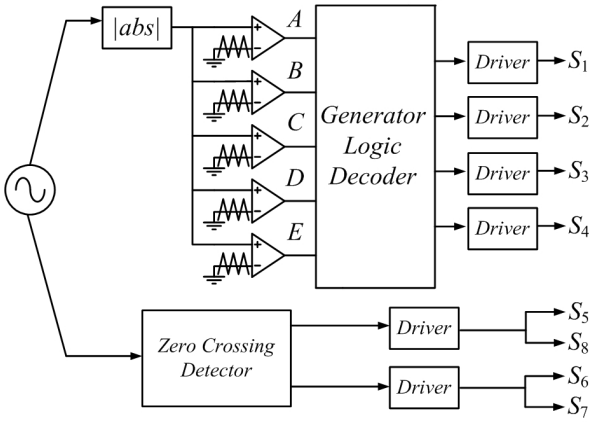


Fig. 2. Control Circuit of the Asymmetrical 11-Level Inverter [17]

C. Boost Charge Control for MPPT

The Boost Converter is integrated with the MPPT for maximizing the power output from the PV cells to the battery. The boost converter with MPPT is shown in Fig 3. The algorithm for the MPPT is described in Equation (8)

$$\left(\frac{dP}{dV}\right)_{MPP} = 0 \tag{8}$$

Based on Equation (8), the control system will always work within these condition:

$$\frac{dP}{dV} > 0,\ if\ \ G > \Delta G \tag{9}$$

$$\frac{dP}{dV} = 0,\ if\ \ G = \Delta G \tag{10}$$

$$\frac{dP}{dV} < 0,\ if\ \ G < \Delta G \tag{11}$$

Fig 3. shows the MPPT control structure based on the characteristic curves and proposed control scheme as shown in Fig 4.

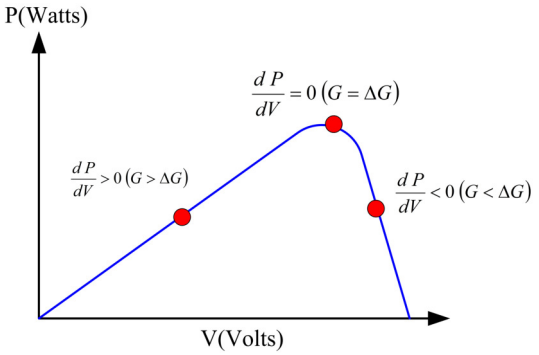


Fig. 3. Maximum Power Point Tracking Curve Based on P & O

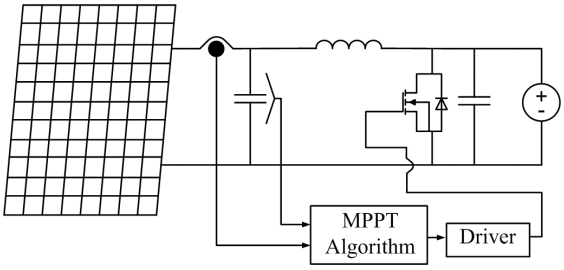


Fig. 4. The Proposed Control Scheme of Boost DC-DC Converter Integrated MPPT

D. Voltage Controller

The circuit design of the asymmetrical 11-level inverter is shown in block diagram seen in Fig 5. By using the *Ziegler-Nichols* method, the Proportional-Integral controller equation for this operation is represented in Equation (12). The Proportional parameter represented as in Equation (13) and Integral parameter represented as in Equation (14).

$$PI_{control} = K_p \left[1 + \frac{1}{\tau_i s}\right] \tag{12}$$

$$K_p = 0,9\ \frac{T}{L} \tag{13}$$

$$\tau_i = \frac{L}{0,3} \quad (14)$$

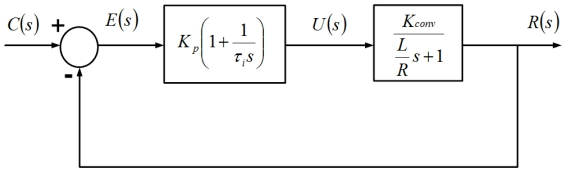


Fig. 5. Block Diagram of the Asymmetrical 11-Level Inverter

III. Results and Discussion

A. Simulation

Simulation results of the proposed inverter design is simulated through PSIM software, the parameters used in this simulation are represented in Table 2.

TABLE II
Simulation Parameters

Parameters	Units
Battery input E	67,5V
Battery input 2E	135V
Inductive Load Filter	2mH
Load Ratings	100W
Measured Inverter Capacity	1500W
Carrier Frequency	5kHz

Processed through the logic decoder, SPWM for the five basic levels constructed are decoded into four logic inputs for switches S_1 – S_4 that are represented through Fig 6.

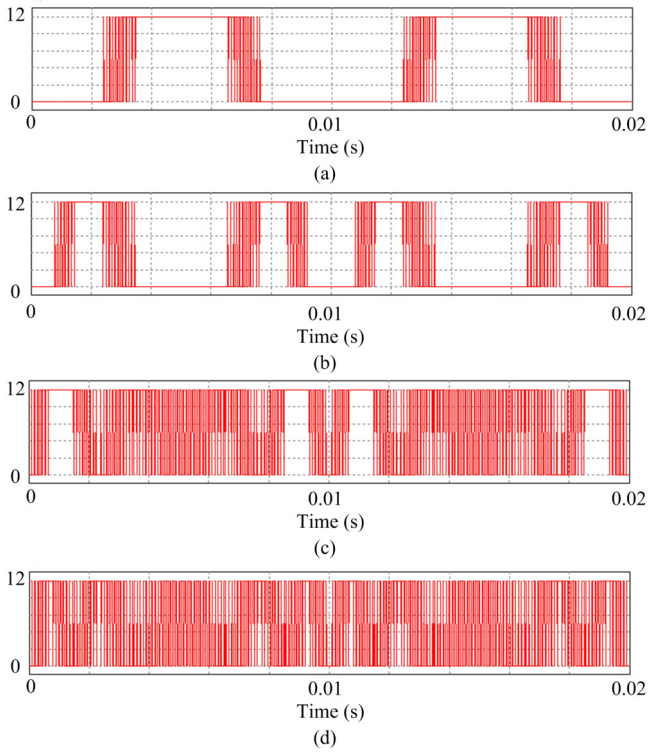


Fig. 6. SPWM Input: (a). S1, (b). S2, (c). S3, (d). S4 [17]

With the Polarity Generator at a half positive cycle constructed seen in Fig 7 (a) and a negative cycle constructed seen in Fig 7 (b). Finally, the result of the 11-level inverter is shown in Fig 7 (c).

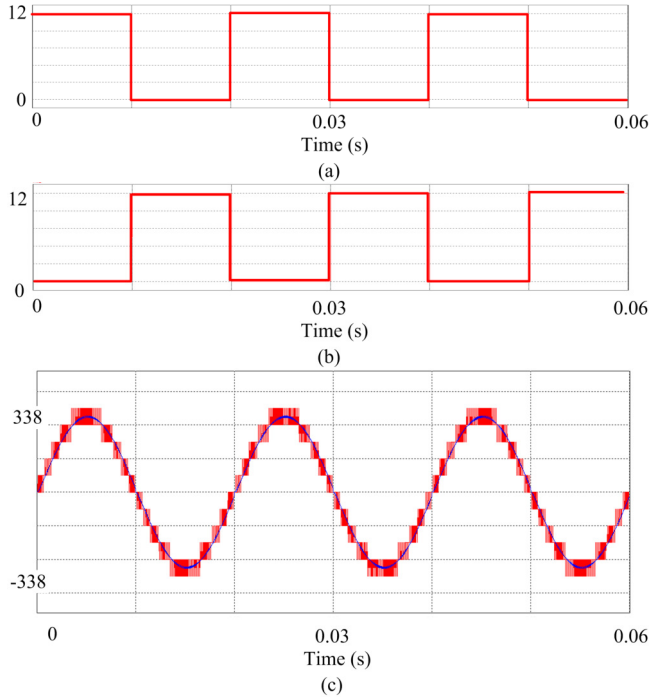
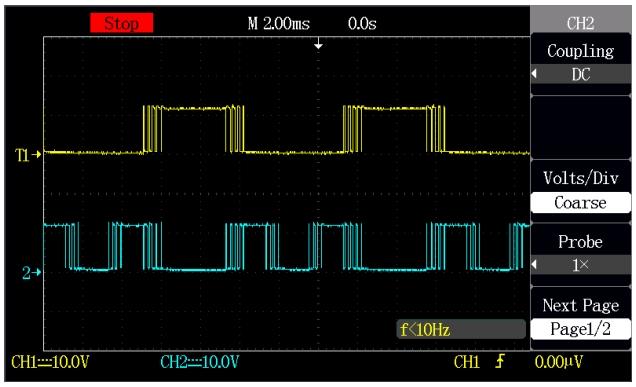


Fig. 7. Output of the 11-Level Inverter: (a). S5 = S8, (b). S6 = S7, (c). The 11-level AC Output Compared with Fundamental Voltage [17]

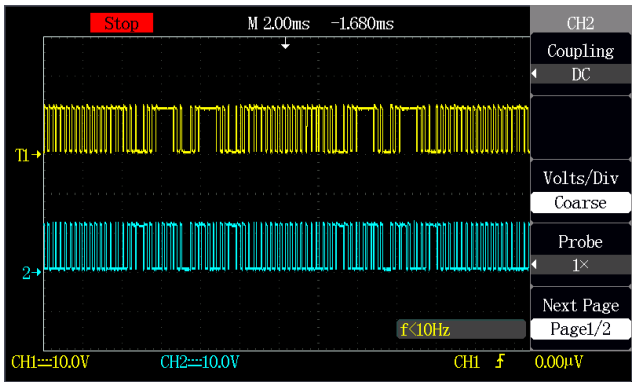
With the aim of achieving the peak voltage 338VAC, The battery input E should be approximately 67,5VDC for the proposed model inverter level generation process. For attaining the 67,5VDC input itself is constructed and regulated through 5 arranged series-connected 13,5VDC batteries. The real-time measured inverter output capacity is recorded 1500W with a load of 15 100W Light-bulbs (Referring to Table 2.). With the output filtered by a 2mH inductor, it produces a pure AC sinusoidal waveform with a 220VAC RMS value for 220VAC/50Hz residential applications.

B. Prototype

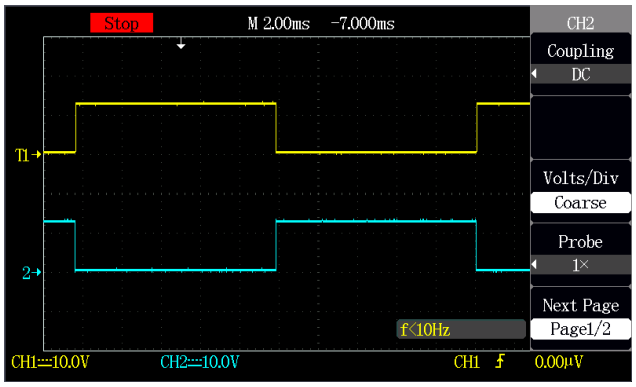
After the simulation analysis is completed, the hardware implementation is tested. Comparing simulation results in Fig 6., with the tested hardware as shown in Fig 8. The decoded inputs for SPWM S_1 – S_4 are shown in Fig 8 (a) and (b). With the polarity generators are shown in Fig 8 (c) for S_5 = S_8, and switches S_6 = S_7.



(a)



(b)



(c)

Fig. 8. SPWM Logic Output Waveform: (a). S1 and S2, (b), S3 and S4, (c) S5 = S8, S6 = S7

The final tests of the hardware implementation analysis results in a construction of the 11-level output waveform as seen on Fig 9.

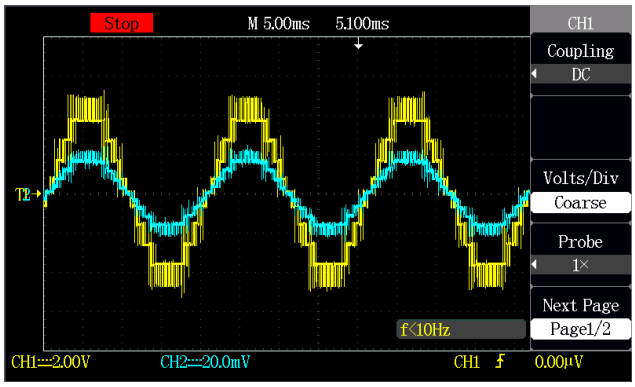


Fig. 9. 11-Level Voltage (yellow) and Current (blue) Output Waveform

The 11-level output waveform is filtered through an inductive filter of 2mH which is seen on Fig 10.

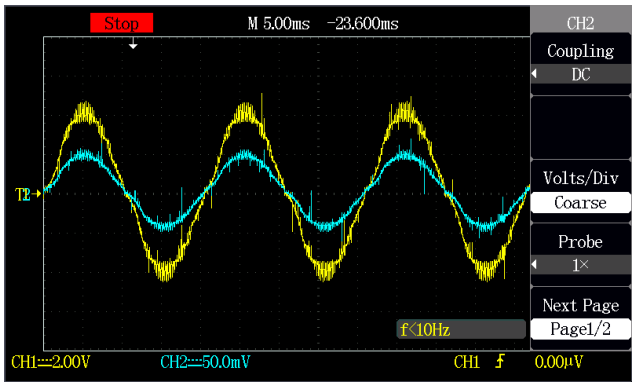


Fig. 10. Filtered 11-Level Output Waveform: Voltage (Yellow) and Current (blue)

Fig 11. shows the current THD values from the FFT analysis scaled by 1: 0.1. Based on Figure 12, a THD_i analysis read values approximately 3.43% for an inductive filtered output at frequency of 50Hz for standalone residential usage.

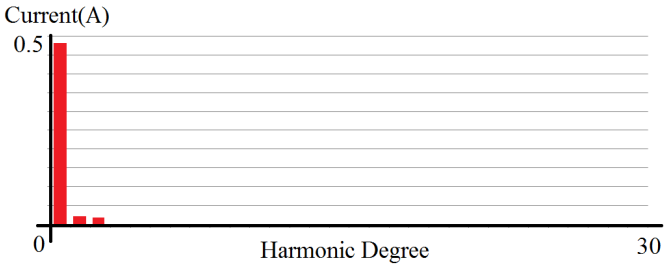


Fig. 11. FFT Analysis from the Output Fundamental Signal

IV. Conclusion

The hardware implementation of the asymmetrical 11-level inverter is conducted in the power conversion laboratory of the Electrical Engineering Department of Soegijapranata Catholic University. The test proved that the asymmetrical 11-level inverter works within expected values. The constructed inverter

hardware implementation itself proves to use fewer number of active power switches compared to conventional constructions which affects the compact structure of the hardware and the current control algorithm dimensions. Laboratory test results in a THD_i value approximately 3.43% for the fundamental current of 4.72A at a base frequency of 50Hz measured with the HIOKI 3286-20 power meter THD record function which is below 5% for 2.3 - 69kV usage IEEE 519 harmonic limits standard.

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