

LAMPIRAN



Current Transducer HX 03 .. 50-P/SP2 $I_{PN} = 3 .. 50 A$

For the electronic measurement of currents: DC, AC, pulsed, mixed, with a galvanic isolation between the primary circuit (high power) and the secondary circuit (electronic circuit).



Electrical data

Primary nominal r.m.s. current I_{PN} (A)	Primary current measuring range I_p (A) ¹⁾	Primary Conductor Diameter x Turns (mm)	Type
3	± 9	0.6d x 20T	HX 03-P/SP2
5	± 15	0.8d x 12T	HX 05-P/SP2
10	± 30	1.1d x 6T	HX 10-P/SP2
15	± 45	1.4d x 4T	HX 15-P/SP2
20	± 60	1.6d x 3T	HX 20-P/SP2
25	± 75	1.6d x 2T	HX 25-P/SP2
50	± 150	1.2 x 6.3 x 1T	HX 50-P/SP2

V_{OUT}	Output voltage @ $\pm I_{PN}$, $R_L = 2 k\Omega$, $T_A = 25^\circ C$	$V_{DE} \pm 0.625$	V
R_{OUT}	Output impedance	< 50	Ω
R_L	Load resistance	≥ 2	$k\Omega$
V_C	Supply voltage ($\pm 5\%$)	+12 .. +15	V
I_C	Current consumption	< 15	mA
V_D	R.m.s. voltage for AC isolation test, 50/60Hz, 1 mn > 3		kV
V_e	R.m.s. voltage for partial discharge extinction at 10pC	≥ 1	kV
	Impulse withstand voltage, 1.2/50 μ s	≥ 6	kV

Accuracy-Dynamic performance data

X	Accuracy @ I_{PN} , $T_A = 25^\circ C$ (without offset)	< ± 1	% of I_{PN}
ϵ_L	Linearity (0 .. $\pm I_{PN}$)	< ± 1	% of I_{PN}
V_{DE}	Electrical offset voltage, $T_A = 25^\circ C$	+2.5V \pm 50	mV
V_{DH}	Hysteresis offset voltage @ $I_p = 0$; after an excursion of $3 \times I_{PN}$	< ± 10	mV
V_{DT}	Thermal drift of V_{DE}	max. ± 1.5	mV/K
$TC\epsilon_G$	Thermal drift of the gain (% of reading)	± 0.1	%/K
t_r	Response time @ 90% of I_p	≤ 3	μ s
f	Frequency bandwidth (-3 dB) ²⁾	50	kHz

General data

T_A	Ambient operating temperature	- 25 .. + 85	$^\circ C$
T_S	Ambient storage temperature	- 25 .. + 85	$^\circ C$
m	Mass	8	g
	Min. internal creepage distance/clearance	≥ 5.5	mm
	Isolation material group	I	
	Standards	EN50178	

Notes: ¹⁾ With $R_L = 2k\Omega$

²⁾ Small signal only to avoid excessive heating of the magnetic core

Features

- Galvanic isolation between primary and secondary circuit
- Hall effect measuring principle
- Isolation voltage 3000V
- Low power consumption
- Extended measuring range ($3 \times I_{PN}$)
- Single supply from +12V to +15V
- Material according to UL94-V0

Advantages

- Low insertion losses
- Easy to mount with automatic handling system
- Small size and space saving
- Only one design for wide current ratings range
- High immunity to external interference.

Applications

- Switched Mode Power Supplies (SMPS)
- AC variable speed drives
- Uninterruptible Power Supplies (UPS)
- Electrical appliances
- Battery supplied applications
- DC motor drives

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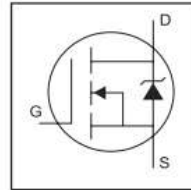
LEM Components

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IRFP250N

HEXFET® Power MOSFET

- Advanced Process Technology
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Ease of Paralleling
- Simple Drive Requirements



$V_{DSS} = 200V$
$R_{DS(on)} = 0.075\Omega$
$I_D = 30A$

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting hole.



Absolute Maximum Ratings

Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	30	A
$I_D @ T_C = 100^\circ C$	21	
I_{DM}	120	W
$P_D @ T_C = 25^\circ C$	214	
	1.4	W/°C
V_{GS}	± 20	V
E_{AS}	315	mJ
I_{AR}	30	A
E_{AR}	21	mJ
dv/dt	8.6	V/ns
T_J	-55 to +175	°C
T_{STG}		
	300 (1.6mm from case)	
	10 lbf•in (1.1N•m)	

Thermal Resistance

Parameter	Typ.	Max.	Units
$R_{\theta JC}$	—	0.7	°C/W
$R_{\theta CS}$	0.24	—	
$R_{\theta JA}$	—	40	

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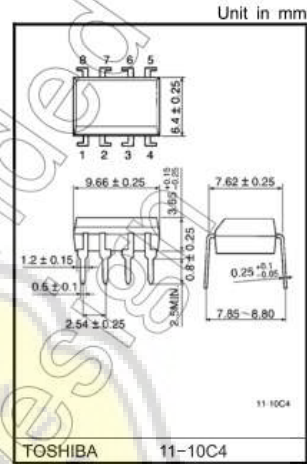
TLP250

Transistor Inverter
 Inverter For Air Conditioner
 IGBT Gate Drive
 Power MOS FET Gate Drive

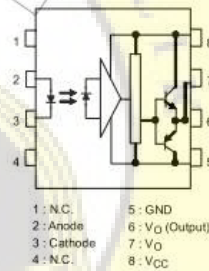
The TOSHIBA TLP250 consists of a GaAlAs light emitting diode and a integrated photodetector.
 This unit is 8-lead DIP package.
 TLP250 is suitable for gate driving circuit of IGBT or power MOS FET.

- Input threshold current: $I_F=5\text{mA}(\text{max.})$
- Supply current (I_{CC}): $11\text{mA}(\text{max.})$
- Supply voltage (V_{CC}): $10\text{--}35\text{V}$
- Output current (I_O): $\pm 1.5\text{A}(\text{max.})$
- Switching time (t_{pLH}/t_{pHL}): $0.5\mu\text{s}(\text{max.})$
- Isolation voltage: $2500V_{\text{rms}}(\text{min.})$
- UL recognized: UL1577, file No.E67349
- Option(D4)
 VDE Approved : DIN EN60747-5-2
 Maximum Operating Insulation Voltage : $890V_{\text{PK}}$
 Highest Permissible Over Voltage : $4000V_{\text{PK}}$

(Note):When a EN60747-5-2 approved type is needed,
 Please designate "Option(D4)"



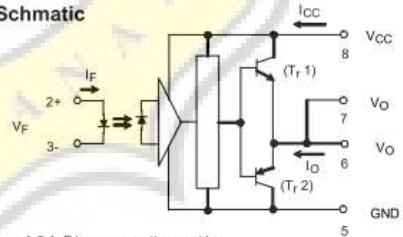
Pin Configuration (top view)



Truth Table

Input LED	Tr1		Tr2	
	On	Off	On	Off
On	On	Off	Off	On
Off	Off	Off	On	Off

Schematic





dsPIC30F4011/4012

dsPIC30F4011/4012 Enhanced Flash 16-bit Digital Signal Controller

Note: This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the *dsPIC30F Family Reference Manual* (DS70046). For more information on the device instruction set and programming, refer to the *dsPIC30F Programmer's Reference Manual* (DS70030).

High Performance Modified RISC CPU:

- Modified Harvard architecture
- C compiler optimized instruction set architecture with flexible addressing modes
- 84 base instructions
- 24-bit wide instructions, 16-bit wide data path
- 48 Kbytes on-chip Flash program space (16K Instruction words)
- 2 Kbytes of on-chip data RAM
- 1 Kbytes of non-volatile data EEPROM
- Up to 30 MIPS operation:
 - DC to 40 MHz external clock input
 - 4 MHz-10 MHz oscillator input with PLL active (4x, 8x, 16x)
- 30 interrupt sources
 - 3 external interrupt sources
 - 8 user selectable priority levels for each interrupt source
 - 4 processor trap sources
- 16 x 16-bit working register array

DSP Engine Features:

- Dual data fetch
- Accumulator write back for DSP operations
- Modulo and Bit-Reversed Addressing modes
- Two, 40-bit wide accumulators with optional saturation logic
- 17-bit x 17-bit single cycle hardware fractional/integer multiplier
- All DSP instructions single cycle
- \pm 16-bit single cycle shift

Peripheral Features:

- High current sink/source I/O pins: 25 mA/25 mA
- Timer module with programmable prescaler:
 - Five 16-bit timers/counters; optionally pair 16-bit timers into 32-bit timer modules
- 16-bit Capture input functions
- 16-bit Compare/PWM output functions
- 3-wire SPI™ modules (supports 4 Frame modes)
- I²C™ module supports Multi-Master/Slave mode and 7-bit/10-bit addressing
- 2 UART modules with FIFO Buffers
- 1 CAN modules, 2.0B compliant

Motor Control PWM Module Features:

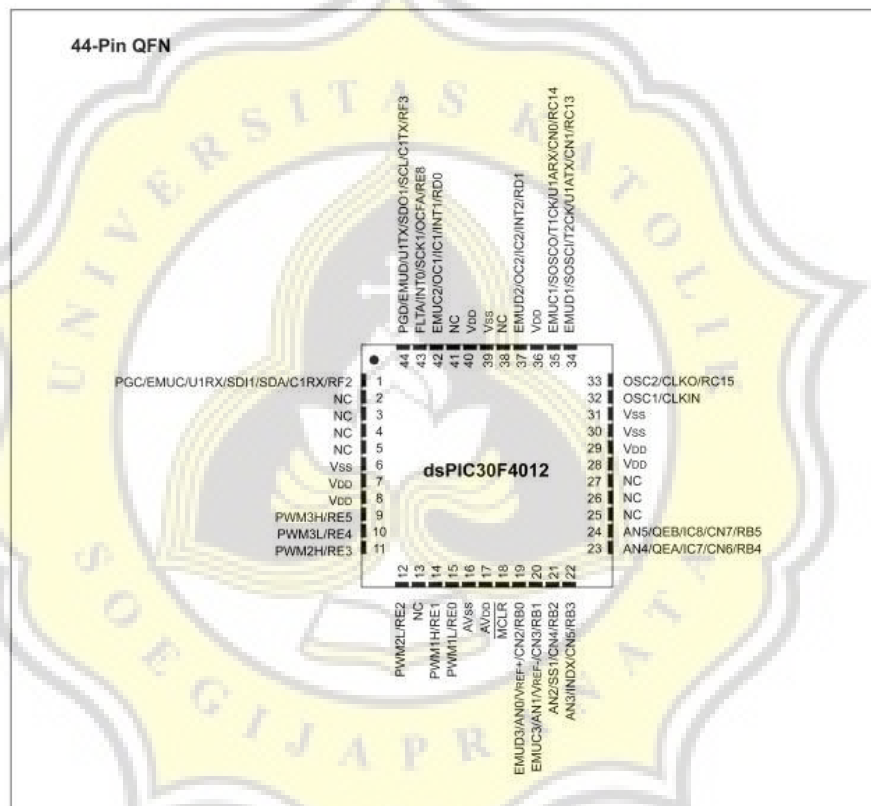
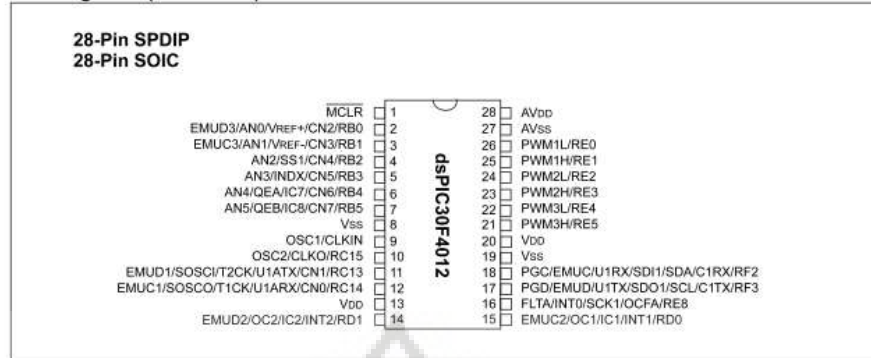
- 6 PWM output channels
 - Complementary or Independent Output modes
 - Edge and Center Aligned modes
- 3 duty cycle generators
- Dedicated time base
- Programmable output polarity
- Dead-time control for Complementary mode
- Manual output control
- Trigger for A/D conversions

Quadrature Encoder Interface Module Features:

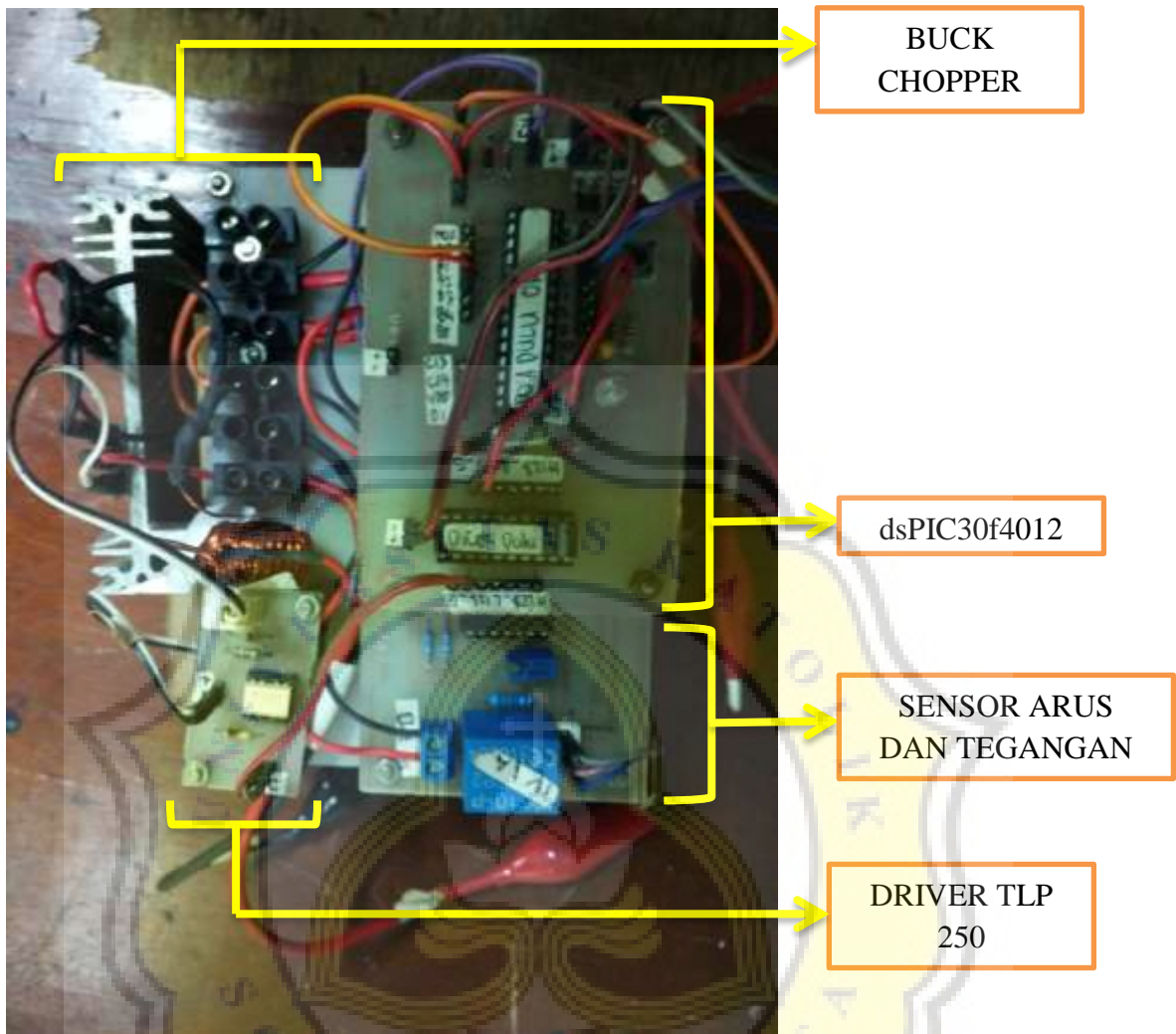
- Phase A, Phase B and Index Pulse input
- 16-bit up/down position counter
- Count direction status
- Position Measurement (x2 and x4) mode
- Programmable digital noise filters on inputs
- Alternate 16-bit Timer/Counter mode
- Interrupt on position counter rollover/underflow

dsPIC30F4011/4012

Pin Diagrams (Continued)



BAGIAN – BAGIAN ALAT



GAMBAR KESULURUHAN ALAT



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